



## Description

### JMT P-channel Enhancement Mode Power MOSFET

#### Features

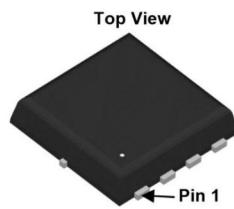
- $V_{DS} = -30V$ ,  $I_D = -40A$
- $R_{DS(ON)} < 9.4m\Omega$  @  $V_{GS} = -10V$
- $R_{DS(ON)} < 15.1m\Omega$  @  $V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free

#### Application

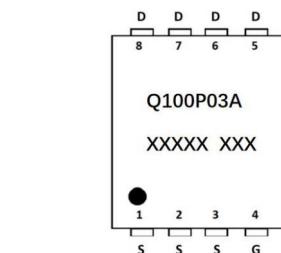
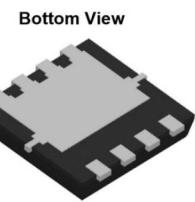
- PWM Applications
- Load Switch
- Power Management



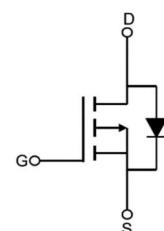
100% UIS TESTED!  
100%  $\Delta V_{ds}$  TESTED!



PDFN3x3-8L



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	Outline	Package	Reel Size	Reel (pcs)	Per Carton (pcs)
Q100P03A	JMTQ100P03A	TAPING	PDFN3x3-8L	13"	5000	50000

## Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
$V_{DSS}$	Drain-Source Voltage		-30	V
$V_{GSS}$	Gate-Source Voltage		$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	-40	A
		$T_C = 100^\circ C$	-26	A
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>		-160	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>		132	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ C$	24	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		5.2	°C/W
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	°C

**Electrical Characteristics** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit s
<b>Off Characteristics</b>						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$ , $I_D = -250\mu\text{A}$	-30	-	-	V
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = -30\text{V}$ , $V_{GS}=0\text{V}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS} = 0\text{V}$ , $V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D = -250\mu\text{A}$	-1.0	-1.6	-2.5	V
$R_{DS(\text{on})}$ note3	Static Drain-Source on-Resistance	$V_{GS} = -10\text{V}$ , $I_D = -20\text{A}$	-	7.5	9.4	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}$ , $I_D = -10\text{A}$	-	11.6	15.1	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{V}$ , $V_{GS}=0\text{V}$ , $f=1.0\text{MHz}$	-	3766	-	pF
$C_{oss}$	Output Capacitance		-	437	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	343	-	pF
$Q_g$	Total Gate Charge	$V_{DD} = -15\text{V}$ , $I_D = -20\text{A}$ , $V_{GS} = -10\text{V}$	-	68	-	nC
$Q_{gs}$	Gate-Source Charge		-	11	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	14	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = -15\text{V}$ , $I_D = -30\text{A}$ , $V_{GS} = -10\text{V}$ , $R_{\text{GEN}} = 2.4\Omega$	-	10	-	ns
$t_r$	Turn-on Rise Time		-	108	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	87	-	ns
$t_f$	Turn-off Fall Time		-	86	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	-40	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	-160	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$ , $I_S = -30\text{A}$	-	-	-1.2	V

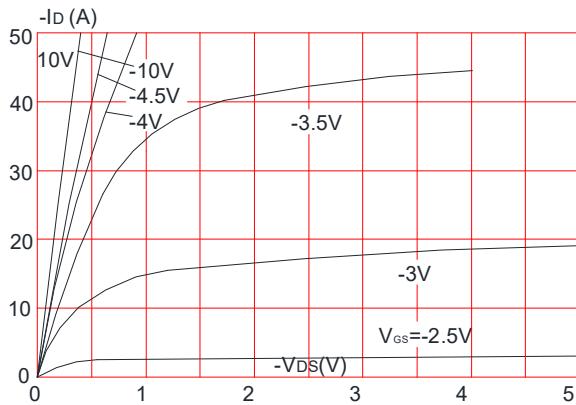
Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: Starting  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = -15\text{V}$ ,  $V_{GS} = -10\text{V}$ ,  $L = 0.5\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = -23\text{A}$

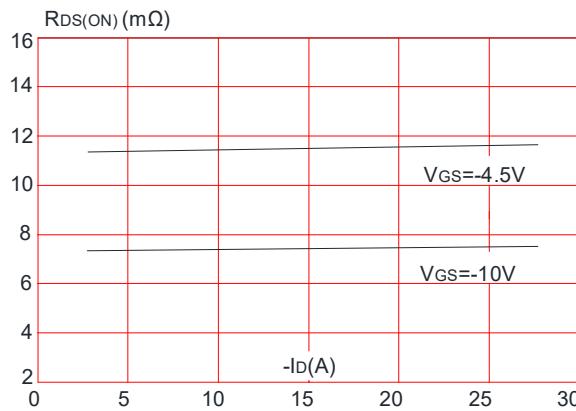
3. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$

## Typical Performance Characteristics

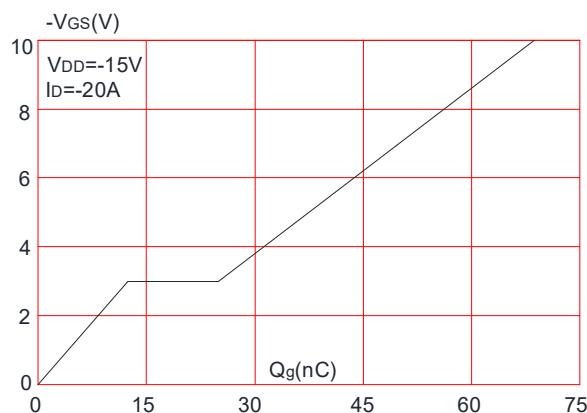
**Figure 1:** Output Characteristics



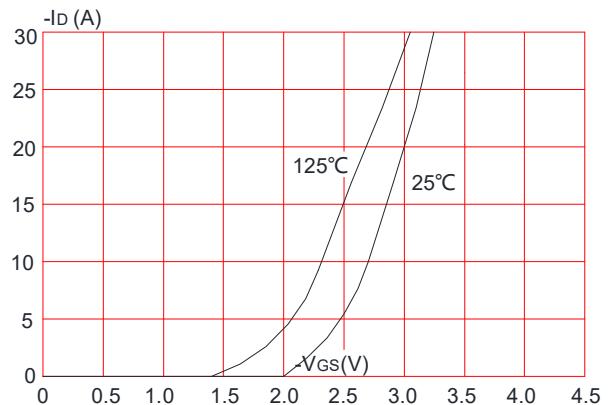
**Figure 3:** On-resistance vs. Drain Current



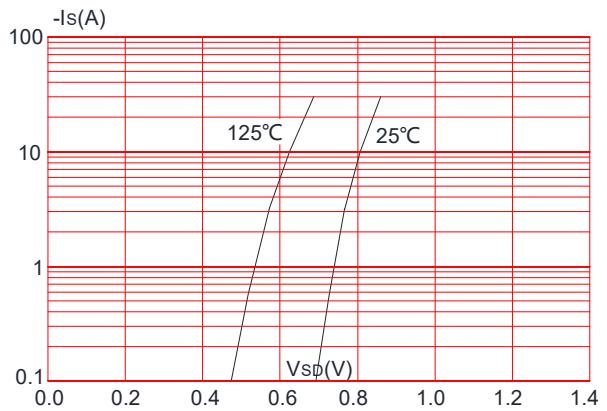
**Figure 5: Gate Charge Characteristics**



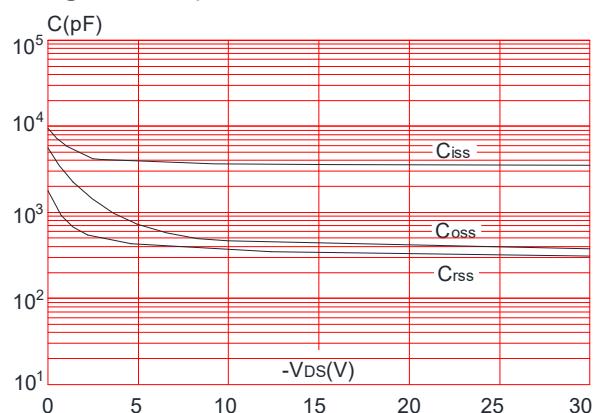
**Figure 2:** Typical Transfer Characteristics



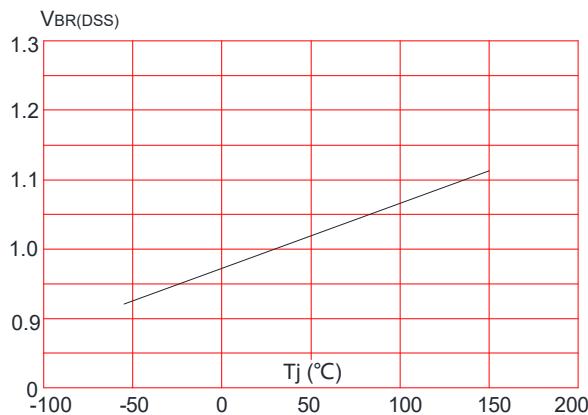
**Figure 4:** Body Diode Characteristics



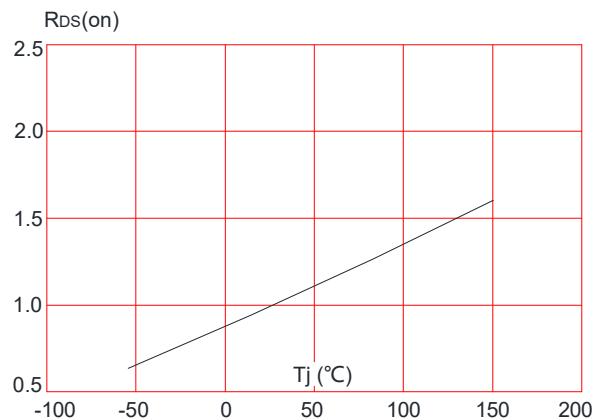
**Figure 6: Capacitance Characteristics**



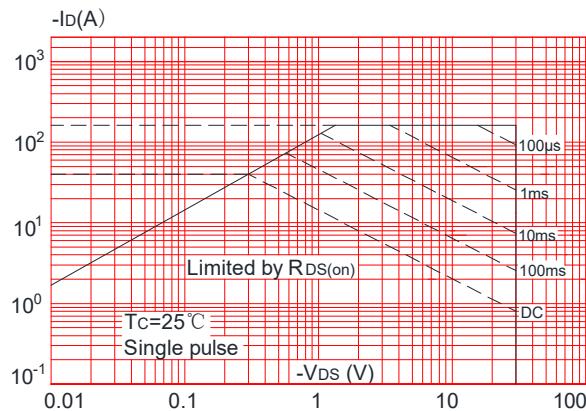
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



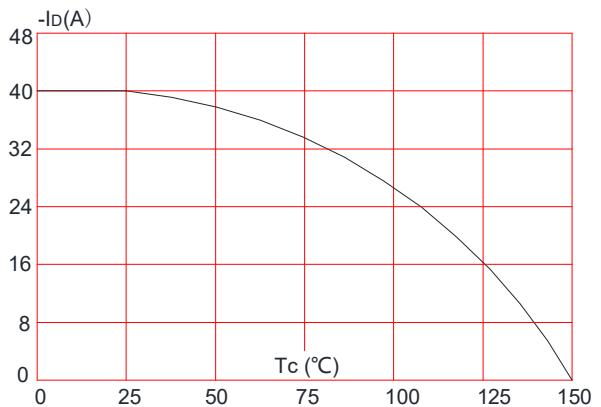
**Figure 8:** Normalized on Resistance vs. Junction Temperature



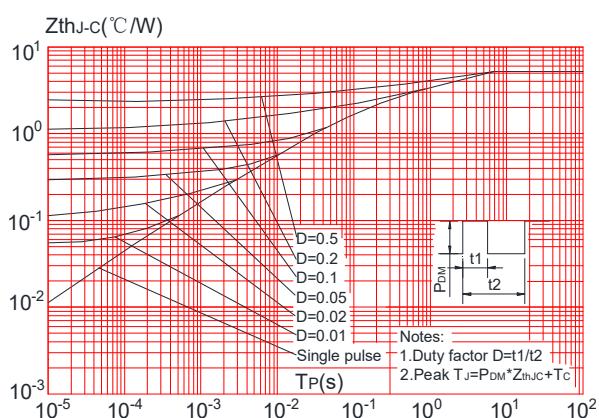
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature

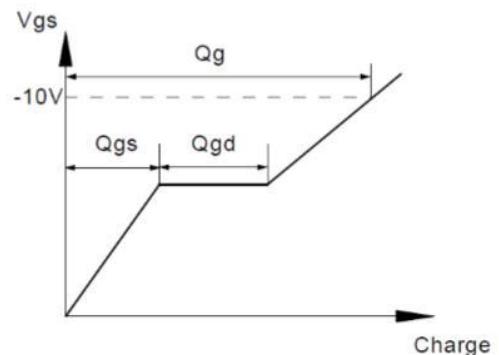
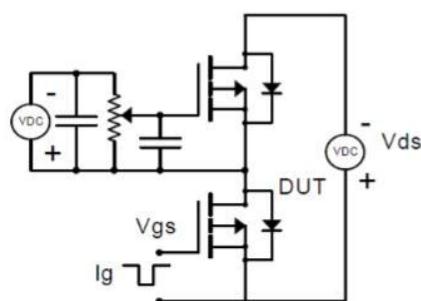


**Figure 11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case

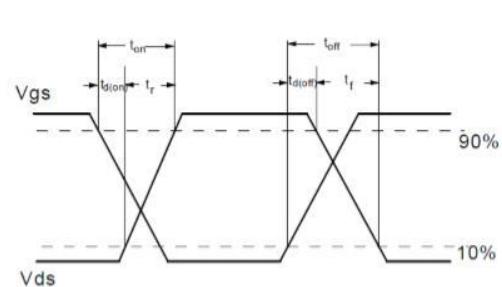
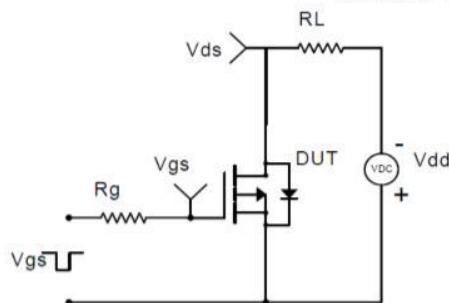


## Test Circuit

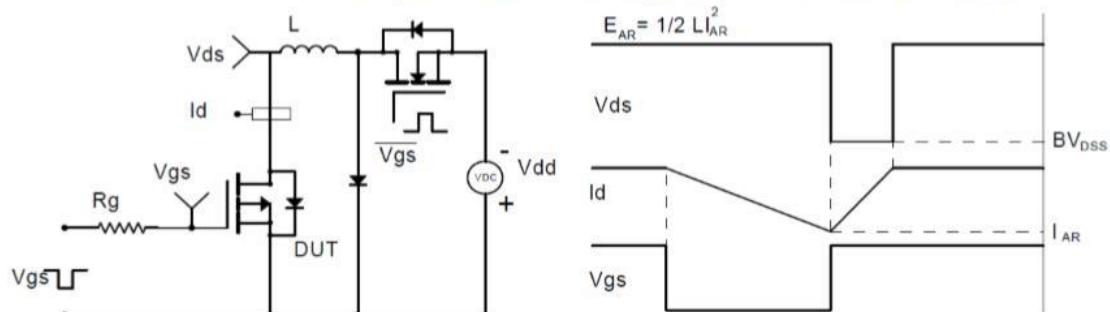
Gate Charge Test Circuit & Waveform



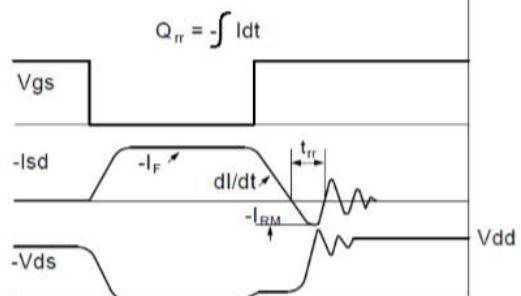
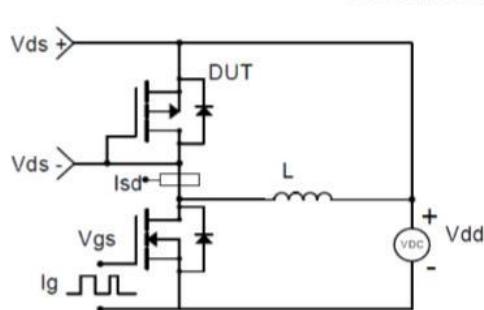
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

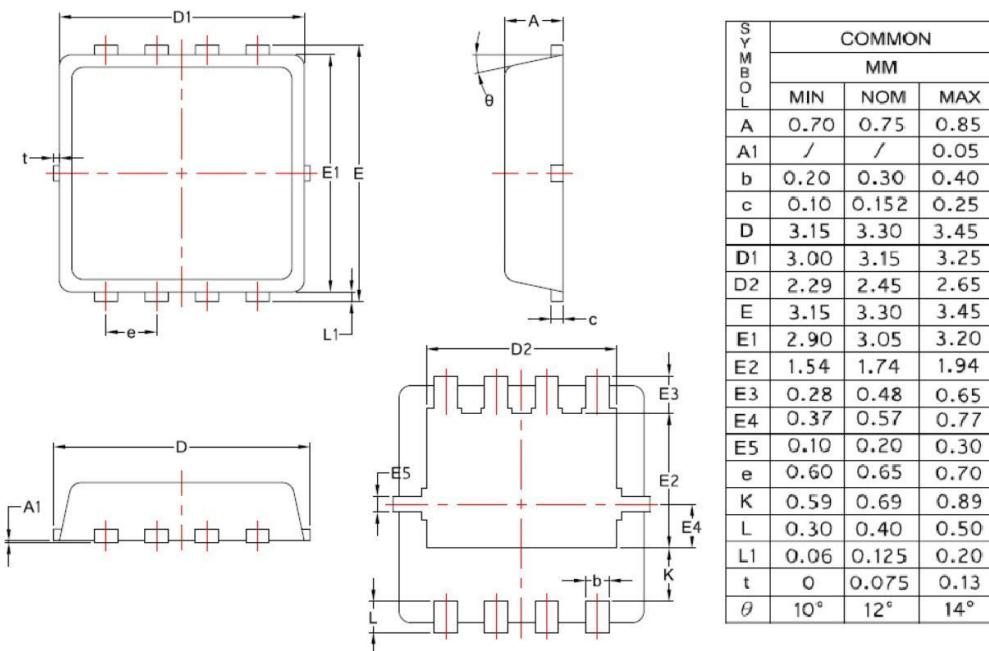


Diode Recovery Test Circuit & Waveforms

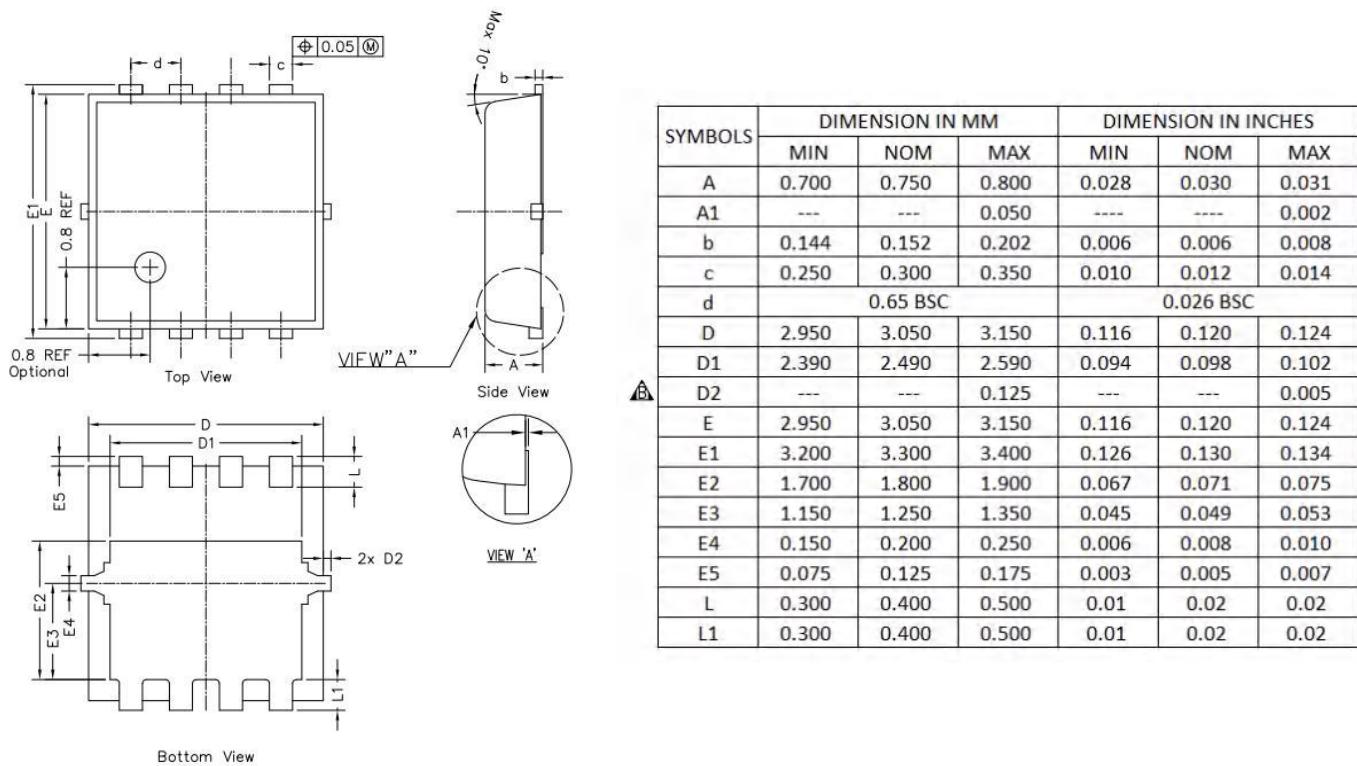




## Package Mechanical Data- PDFN3x3-8L-Type A



## Package Mechanical Data- PDFN3x3-8L-Type B





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