



Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

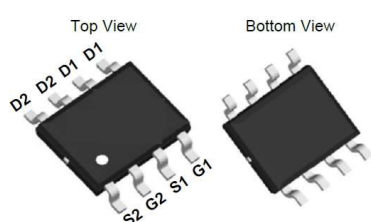
- 40V, 13A
 $R_{DS(ON)} < 12.5m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)} < 18m\Omega$ @ $V_{GS} = 4.5V$
- Lead free and Green Device Available
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

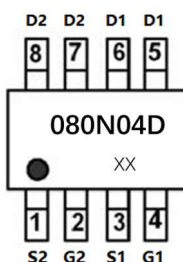
- Load Switch
- PWM Application
- Power management



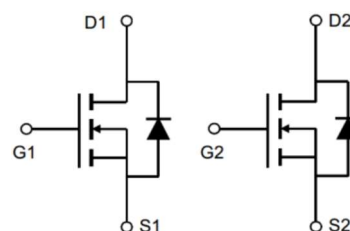
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8(Dual)



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
080N04D	JMTP080N04D	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	13	A
		$T_A = 100^\circ\text{C}$	8.5	A
I_{DM}	Pulsed Drain Current ^{note1}		52	A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}		81	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	4	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		31.3	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.1	1.5	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} =10V, I _D =13A	-	9.6	12.5	mΩ
		V _{GS} =4.5V, I _D =10A	-	13	18	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1.0MHz	-	2400	-	pF
C _{oss}	Output Capacitance		-	192	-	pF
C _{rss}	Reverse Transfer Capacitance		-	165	-	pF
Q _g	Total Gate Charge	V _{DS} =20V, I _D =10A, V _{GS} =10V	-	37	-	nC
Q _{gs}	Gate-Source Charge		-	6	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	7	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} =20V, I _D =10A, R _L =1Ω, R _{GEN} =3Ω, V _{GS} =10V	-	12	-	ns
t _r	Turn-on Rise Time		-	12	-	ns
t _{d(off)}	Turn-off Delay Time		-	38	-	ns
t _f	Turn-off Fall Time		-	9	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	13	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	52	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =13A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	T _J =25℃, I _F =13A,dI/dt=100A/μs	-	22	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	11	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25°C, V_{GS}=10V, R_G=25Ω, L=0.5mH, I_{AS}=18A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure1: Output Characteristics

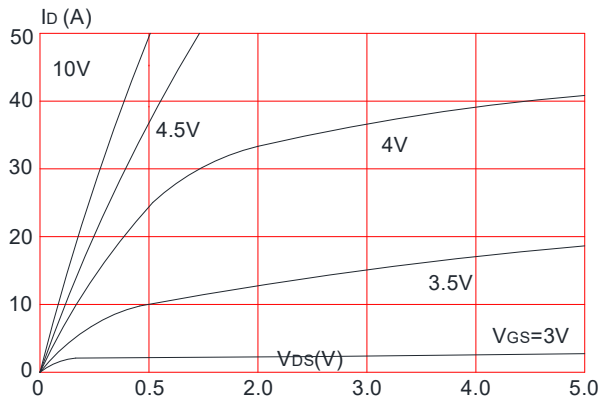


Figure 2: Typical Transfer Characteristics

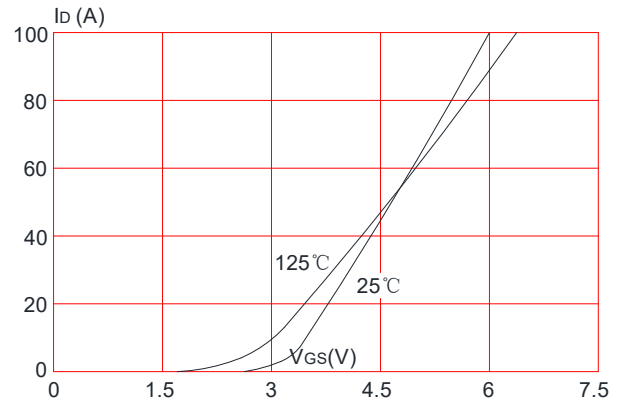


Figure 3: On-resistance vs. Drain Current

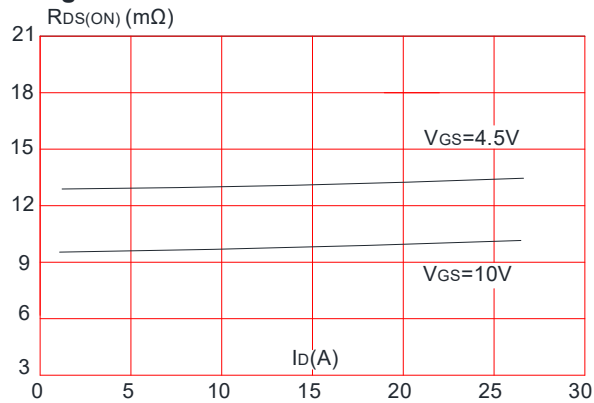


Figure 4: Body Diode Characteristics

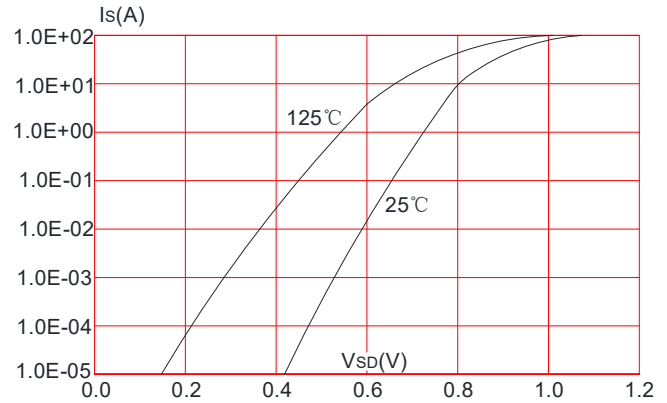


Figure 5: Gate Charge Characteristics

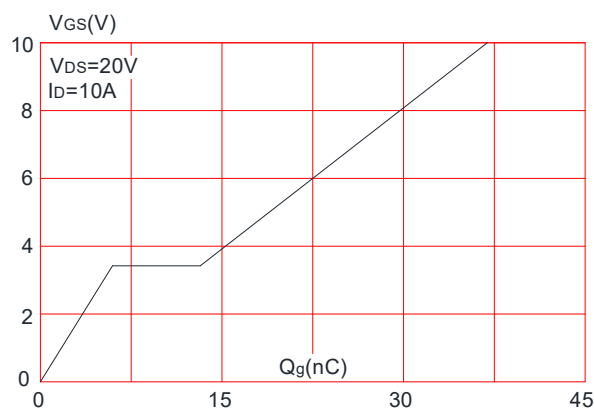


Figure 6: Capacitance Characteristics

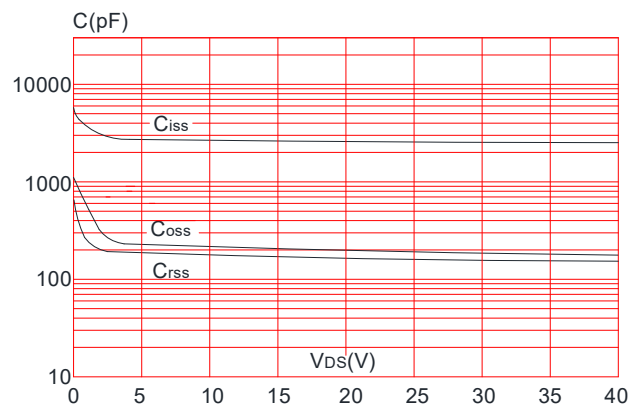


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

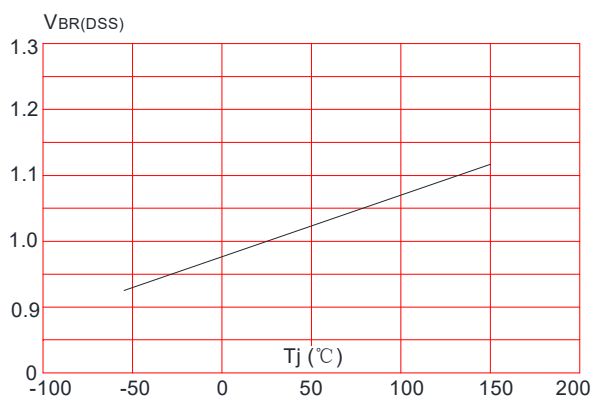


Figure 8: Normalized on Resistance vs. Junction Temperature

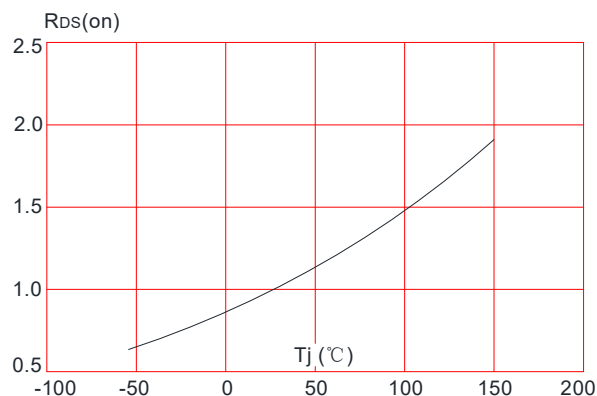


Figure 9: Maximum Safe Operating Area

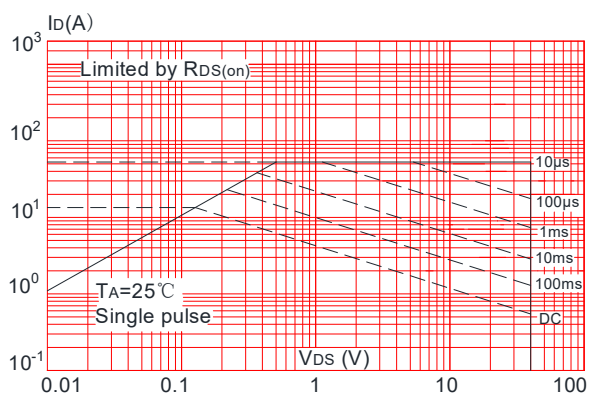


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

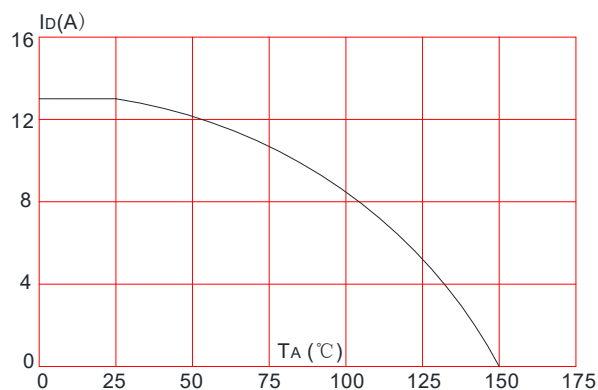
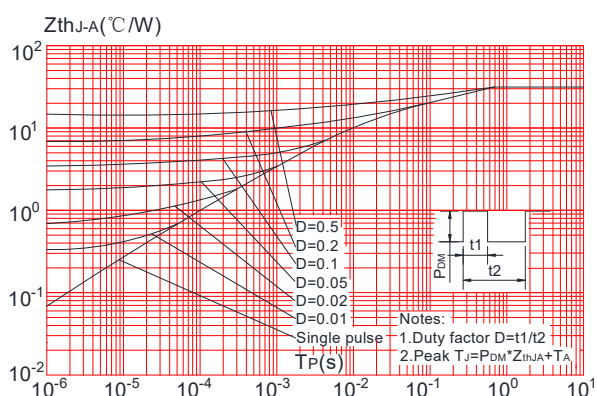


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

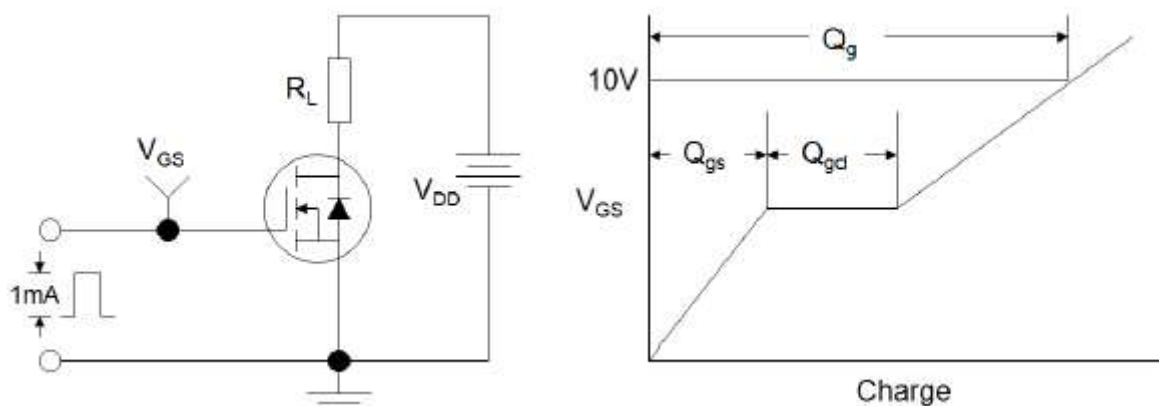


Figure1:Gate Charge Test Circuit & Waveform

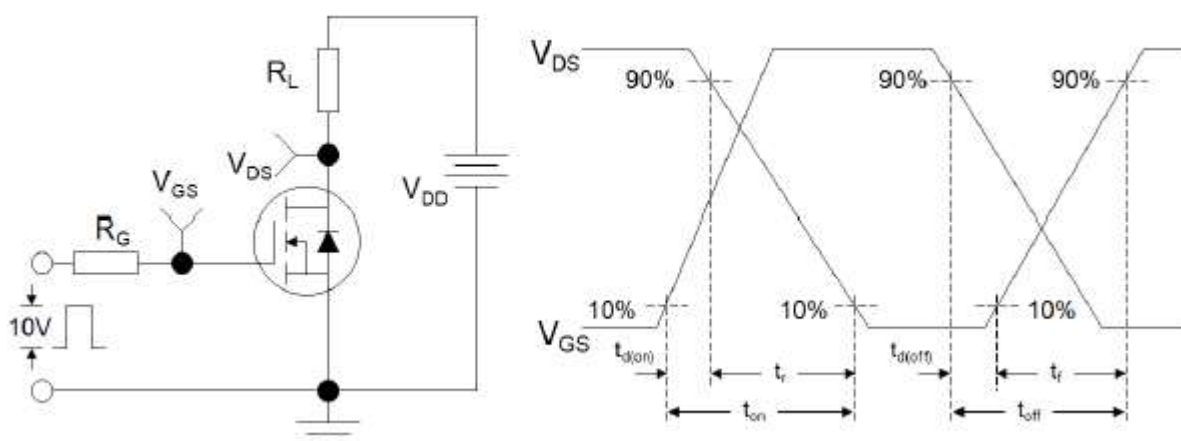


Figure 2: Resistive Switching Test Circuit & Waveforms

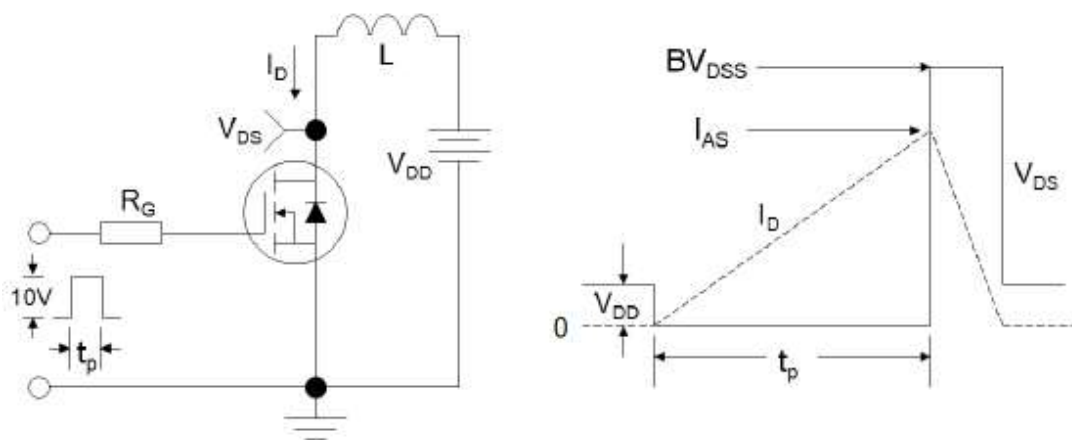
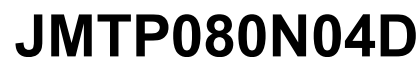
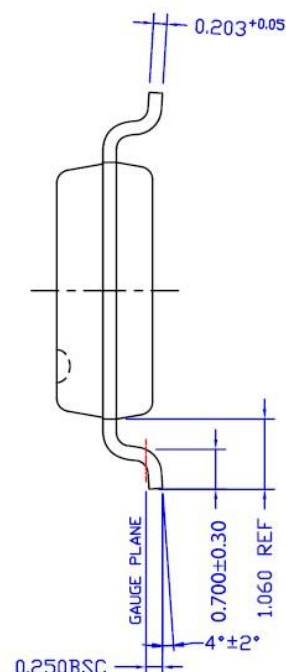
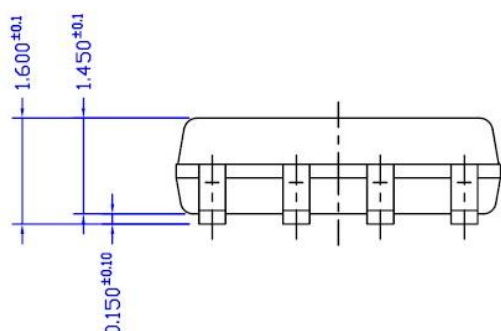


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Technical drawing of a rectangular component with dimensions and tolerances:

- Overall width: 4.900 ± 0.100
- Overall height: 6.000 ± 0.200
- Top edge feature width: 1.270BSC
- Top edge feature spacing: $0.400 \pm 0.05 \sim 8 \times$
- Bottom edge feature width: 1.270BSC
- Bottom edge feature spacing: $0.400 \pm 0.05 \sim 8 \times$
- Internal width: 3.880 ± 0.100
- Internal height: 4.900 ± 0.100



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