



Description

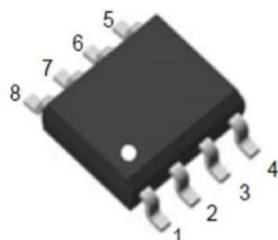
JMT P-channel Enhancement Mode Power MOSFET

Features

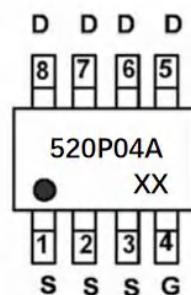
- $V_{DS} = -40V$, $I_D = -5.5A$
- $R_{DS(ON)} < 51 \text{ m}\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} < 78 \text{ m}\Omega @ V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

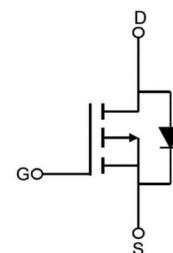
- PWM Applications
- Load Switch
- Power Management



SOP-8 top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
520P04A	JMTP520P04A	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		-40	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	-5.5	A
		$T_A = 100^\circ\text{C}$	-3.6	A
I_{DM}	Pulsed Drain Current ^{note1}		22	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	2.6	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		48	$^\circ\text{C}/\text{W}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$

**Electrical Characteristics** ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D = -250\mu\text{A}$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -40\text{V}$, $V_{GS}=0\text{V}$	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D = -250\mu\text{A}$	-1.0	-1.6	-2.5	V
$R_{DS(\text{on})}$ Note2	Static Drain-Source on-Resistance	$V_{GS} = -10\text{V}$, $I_D = -5\text{A}$	-	39	51	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}$, $I_D = -4\text{A}$	-	56	78	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -20\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	869	-	pF
C_{oss}	Output Capacitance		-	94	-	pF
C_{rss}	Reverse Transfer Capacitance		-	69	-	pF
Q_g	Total Gate Charge	$V_{DS} = -20\text{V}$, $I_D = -4\text{A}$, $V_{GS} = -10\text{V}$	-	17.3	-	nC
Q_{gs}	Gate-Source Charge		-	3.2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	4.3	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DS} = -20\text{V}$, $I_D = -4\text{A}$, $V_{GS} = -10\text{V}$, $R_{\text{GEN}}=3\Omega$	-	10.3	-	ns
t_r	Turn-on Rise Time		-	4.3	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	39	-	ns
t_f	Turn-off Fall Time		-	46.5	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward Current	-	-	-5.5	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	-22	-	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0\text{V}$, $I_s = -5.5\text{A}$	-	-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS}=0\text{V}$, $I_s = -5.5\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$	-	17	-	ns
Q_{rr}	Reverse Recovery Charge		-	11.5	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

Typical Performance Characteristics

Figure 1: Output Characteristics

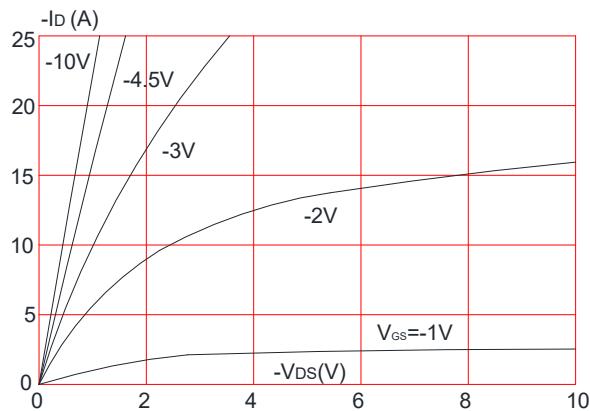


Figure 3: On-resistance vs. Drain Current

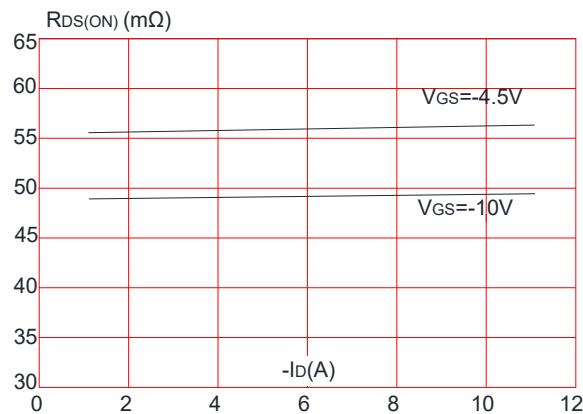


Figure 5: Gate Charge Characteristics

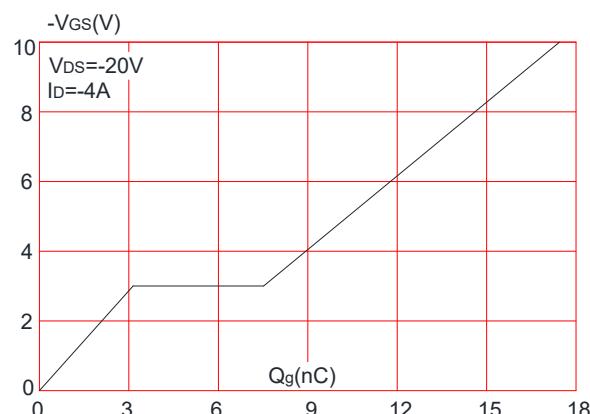


Figure 2: Typical Transfer Characteristics

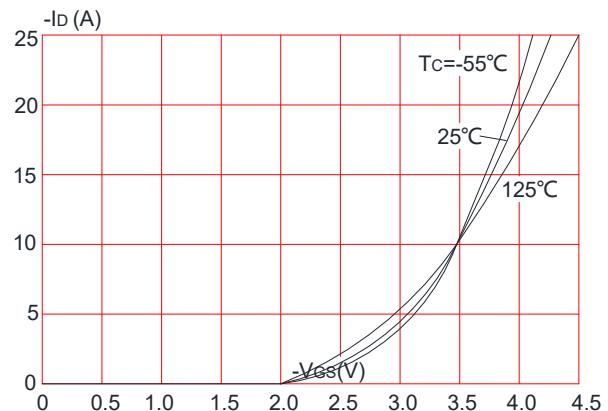


Figure 4: Body Diode Characteristics

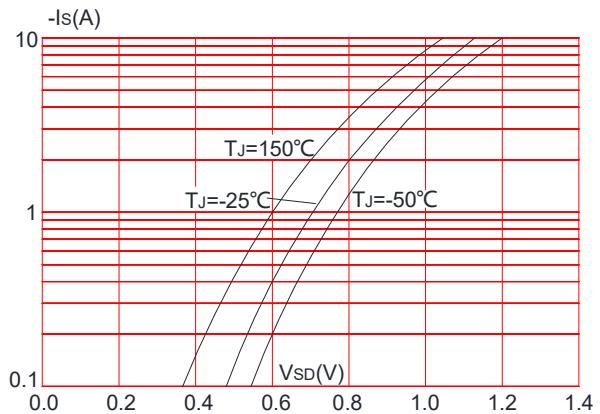


Figure 6: Capacitance Characteristics

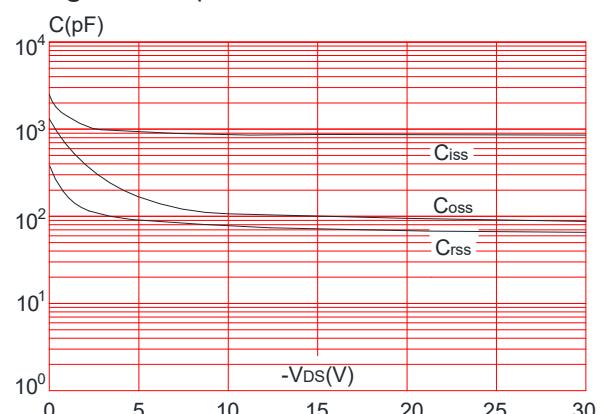


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

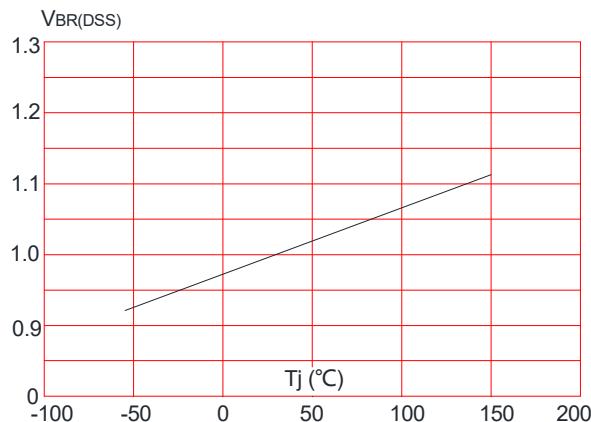


Figure 9: Maximum Safe Operating Area

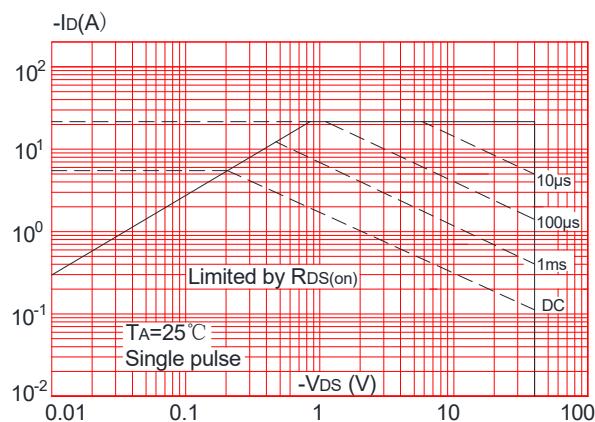


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

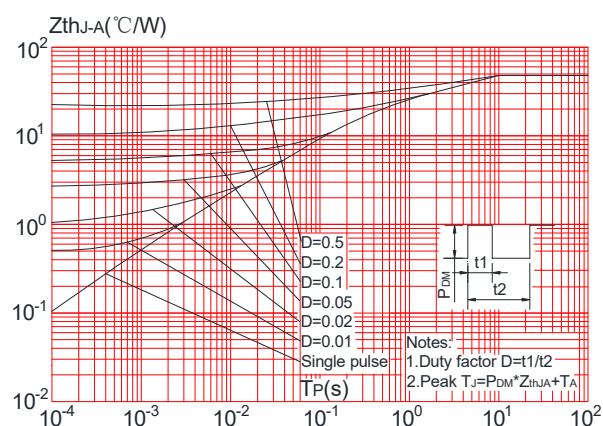


Figure 8: Normalized on Resistance vs. Junction Temperature

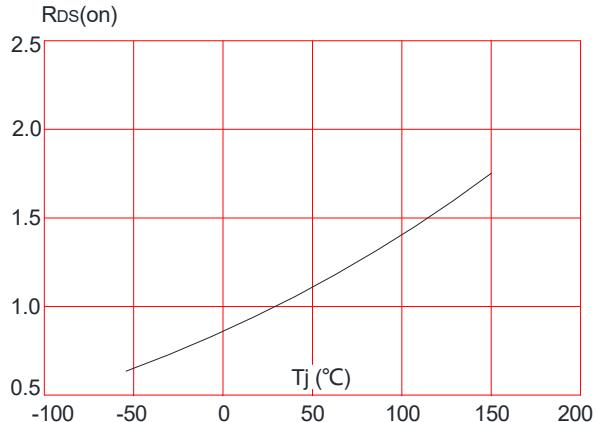
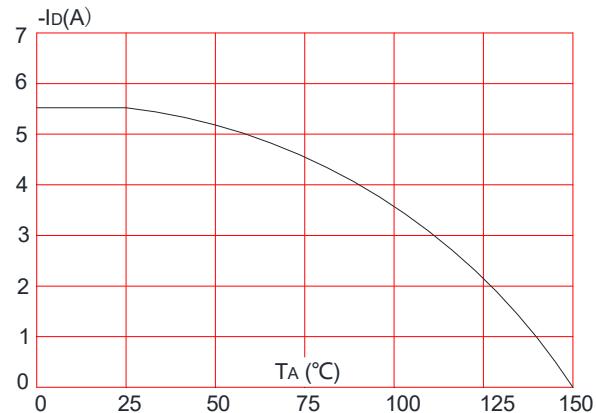
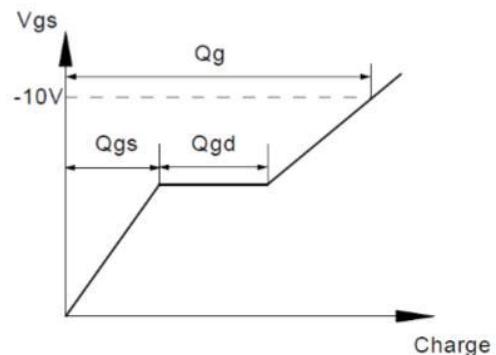
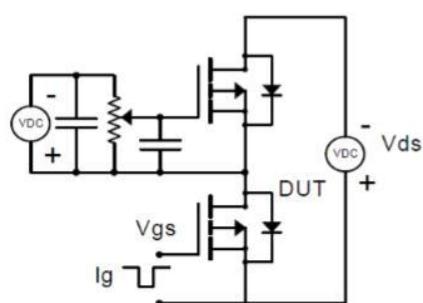


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

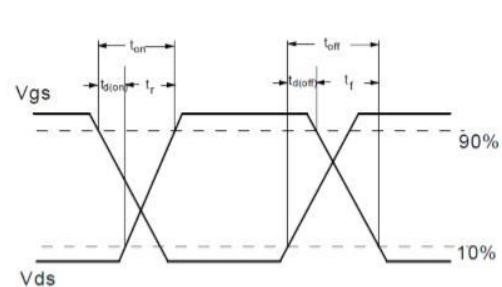
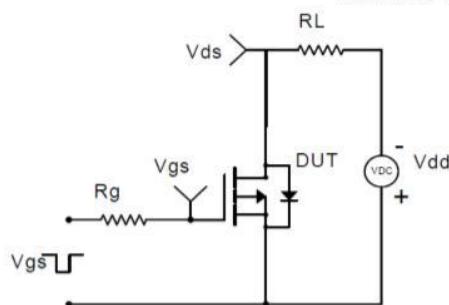


Test Circuit

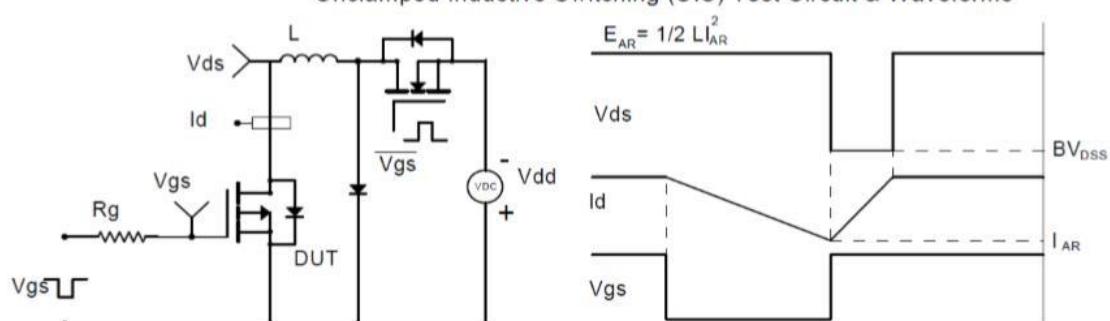
Gate Charge Test Circuit & Waveform



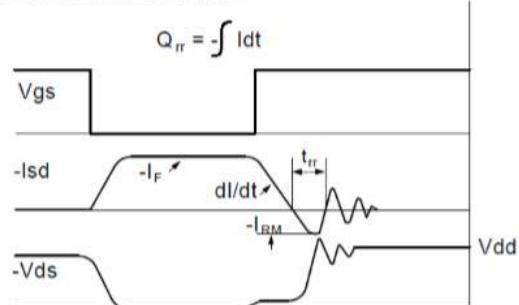
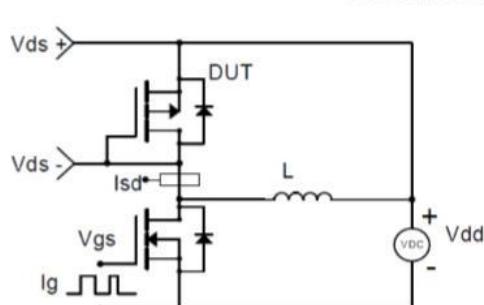
Resistive Switching Test Circuit & Waveforms



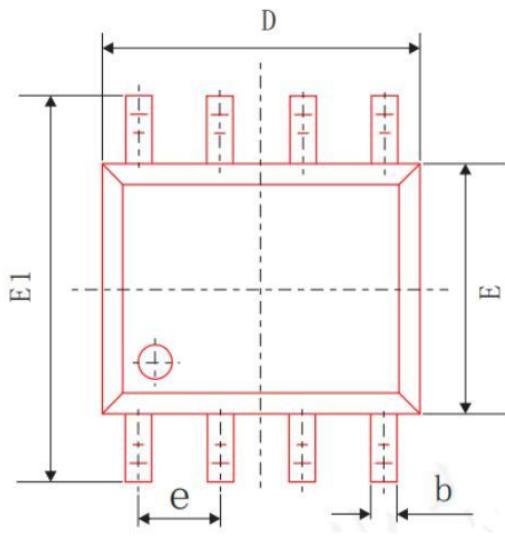
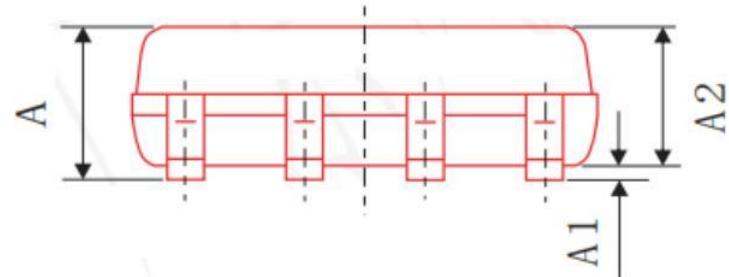
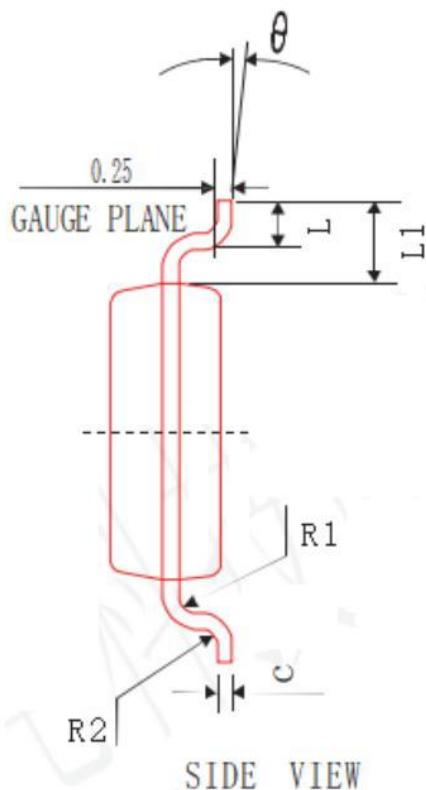
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data- SOP-8

TOP VIEWSIDE VIEW

SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
θ	2°	4°	6°
L1		1.04 REF	
e		1.27 BSC	
R1		0.07 TYP	
R2		0.07 TYP	



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