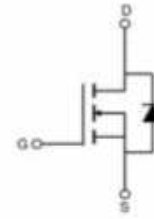


# AP50N04Q

## N-Channel Enhancement Mosfet

### Feature

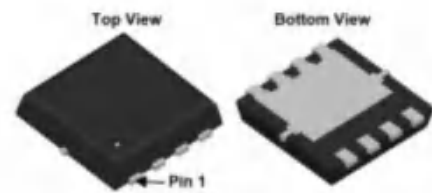
- 40V,20A  
 $R_{DS(on)} < 13m\Omega @ V_{GS}=10V$   
 $R_{DS(on)} < 20m\Omega @ V_{GS}=4.5V$
- Advanced Trench Technology
- Lead free product is acquired
- Excellent  $R_{DS(on)}$  and Low Gate Charge



Schematic Diagram

### Application

- PWM applications
- Load Switch
- Power management



PDFN3.3X3.3-8L

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
50N04Q	AP50N04Q	PDFN3X3-8L	13 inch	-	5000

### ABSOLUTE MAXIMUM RATINGS ( $T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current ( $T_a = 25^\circ\text{C}$ )	$I_D$	20	A
Continuous Drain Current ( $T_a = 100^\circ\text{C}$ )	$I_D$	14	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	60	A
Singel Pulsed Avalanche Energy <sup>(2)</sup>	$E_{AS}$	12.25	mJ
Power Dissipation	$P_D$	35	W
Thermal Resistance from Junction to Case <sup>(4)</sup>	$R_{\theta JC}$	3.6	$^\circ\text{C/W}$
Junction Temperature	$T_J$	150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-55~ +150	$^\circ\text{C}$

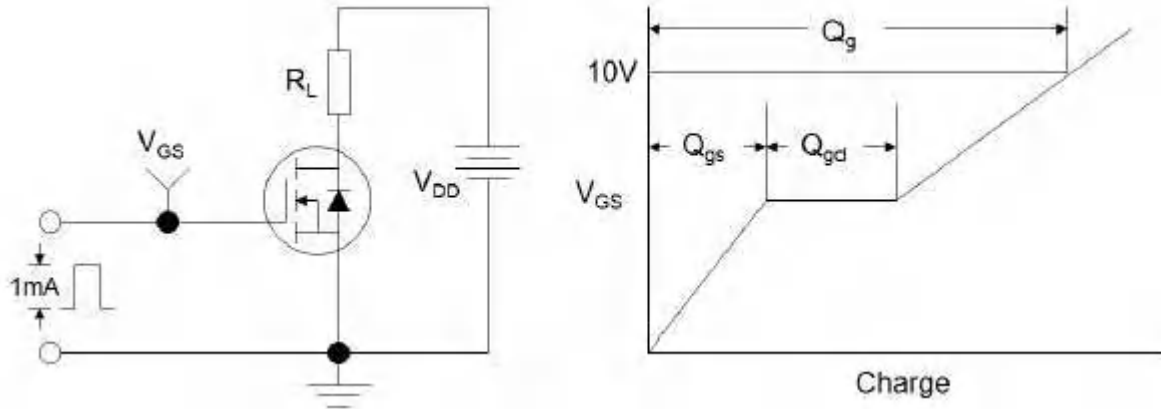
**MOSFET ELECTRICAL CHARACTERISTICS(T<sub>a</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
<b>Static Characteristics</b>						
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	40	-	-	V
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> = 0V	-	-	1	μA
Gate-body leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> = 0V	-	-	±100	nA
Gate threshold voltage <sup>(3)</sup>	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.5	2.5	V
Drain-source on-resistance <sup>(3)</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	10	13	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	13	20	
<b>Dynamic characteristics</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f =1MHz	-	1250	-	pF
Output Capacitance	C <sub>oss</sub>		-	114	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	85	-	
<b>Switching characteristics</b>						
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, I <sub>D</sub> =1A, R <sub>L</sub> =6Ω V <sub>GS</sub> =10V, R <sub>G</sub> =1Ω	-	10	-	ns
Turn-on rise time	t <sub>r</sub>		-	9	-	
Turn-off delay time	t <sub>d(off)</sub>		-	32	-	
Turn-off fall time	t <sub>f</sub>		-	16	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =20V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V	-	20	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	3.5	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	4.2	-	
<b>Source-Drain Diode characteristics</b>						
Diode Forward voltage <sup>(3)</sup>	V <sub>DS</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-	-	1.2	V
Diode Forward current <sup>(4)</sup>	I <sub>S</sub>		-	-	40	A

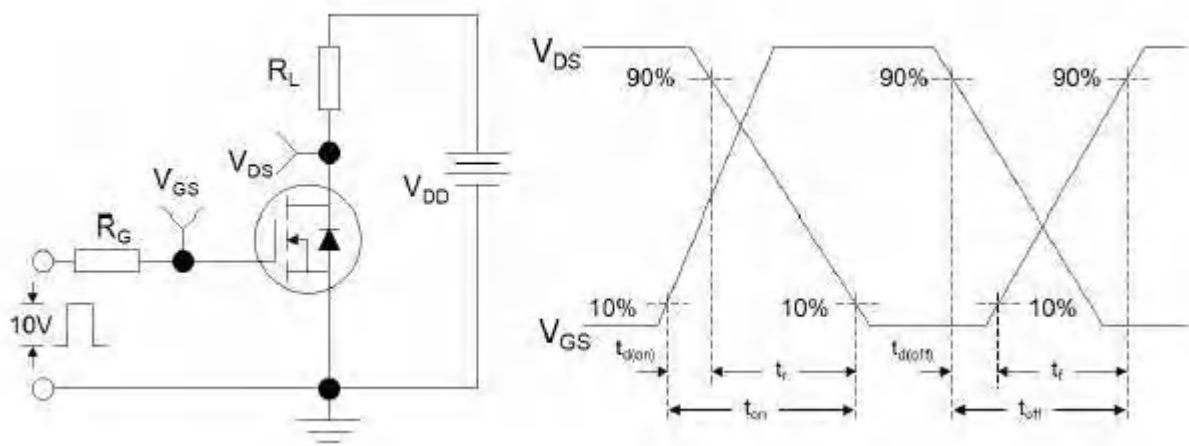
**Notes:**

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=20V, R<sub>G</sub>=25 Ω, L=0.5mH, I<sub>AS</sub>= 7A
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board, t≤10 sec

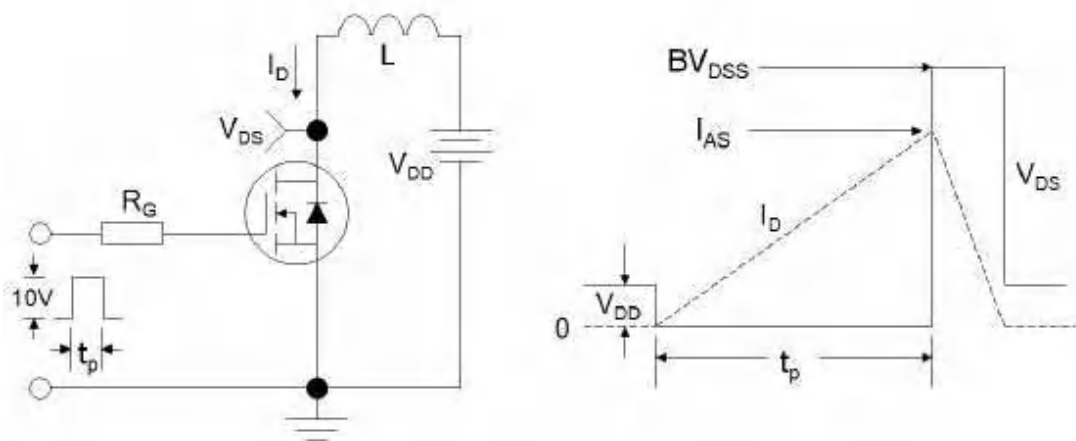
**Test Circuit**



**Figure 1: Gate Charge Test Circuit & Waveform**



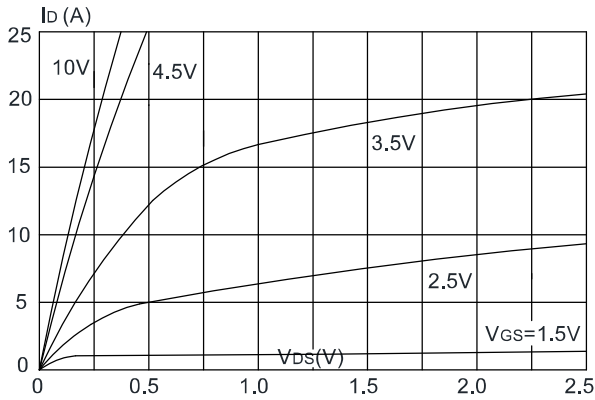
**Figure 2: Resistive Switching Test Circuit & Waveforms**



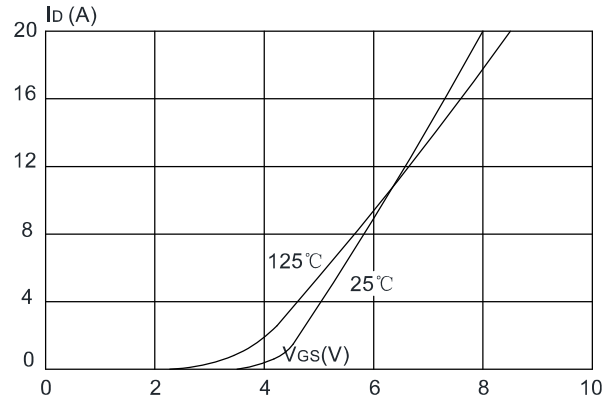
**Figure 3: Unclamped Inductive Switching Test Circuit & Waveforms**

**Typical Performance Characteristics**

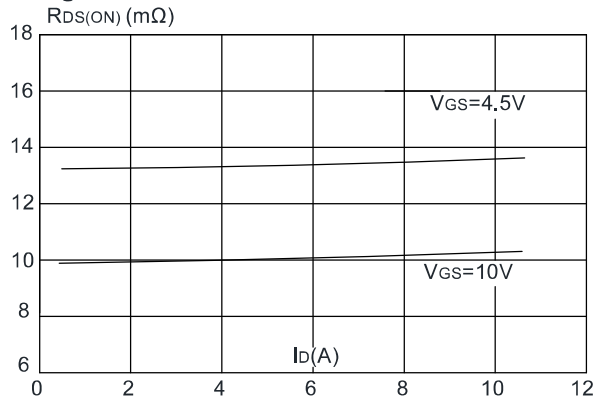
**Figure 1: Output Characteristics**



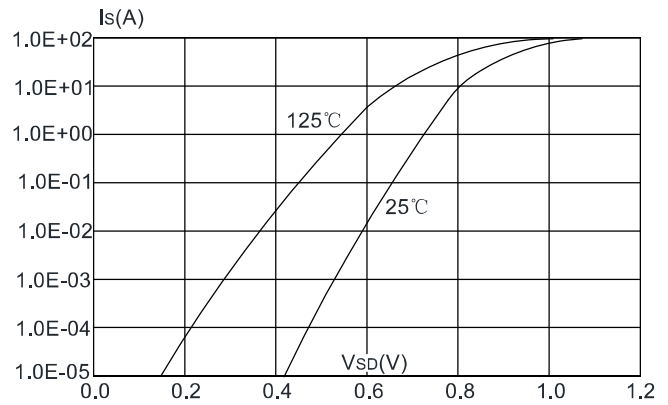
**Figure 2: Typical Transfer Characteristics**



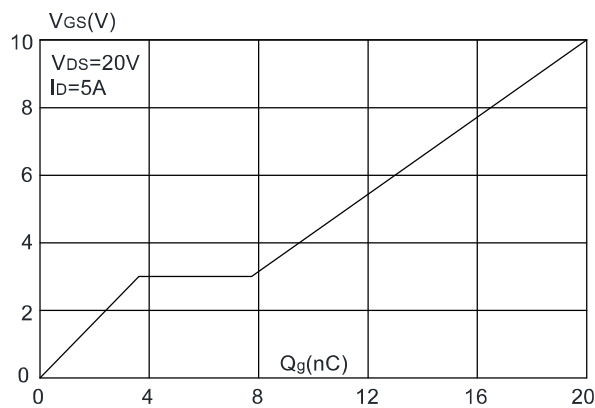
**Figure 3: On-resistance vs. Drain Current**



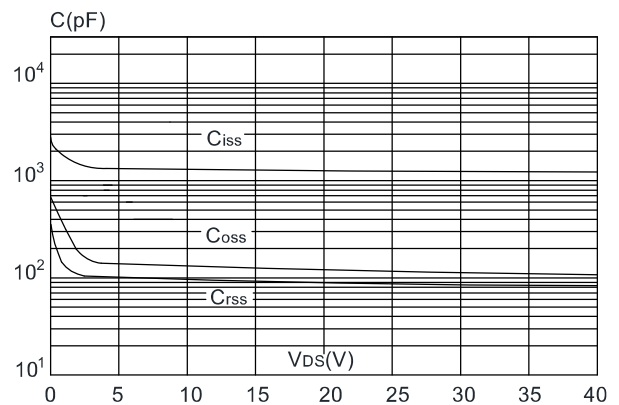
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**



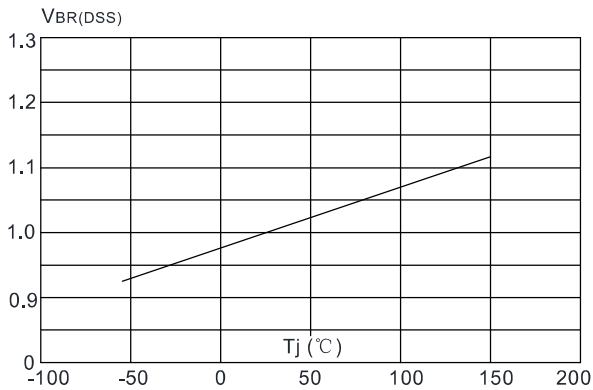
**Figure 6: Capacitance Characteristics**



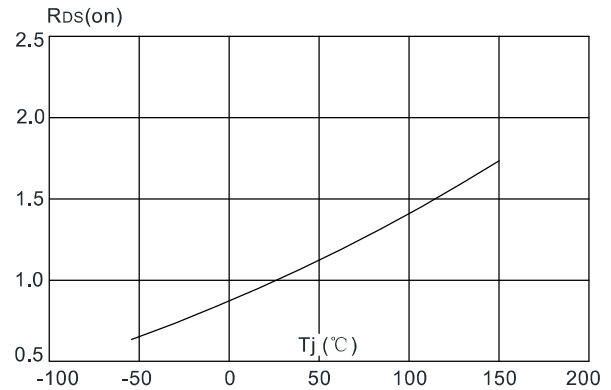
# AP50N04Q

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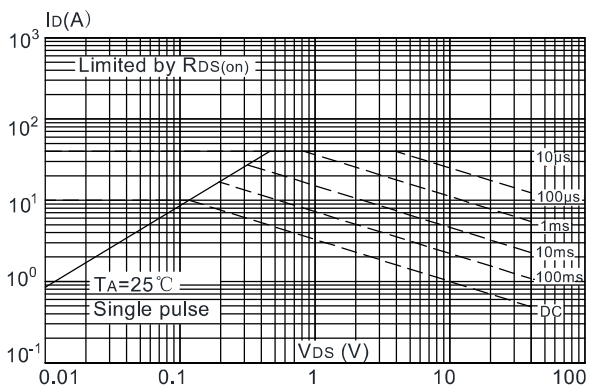
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



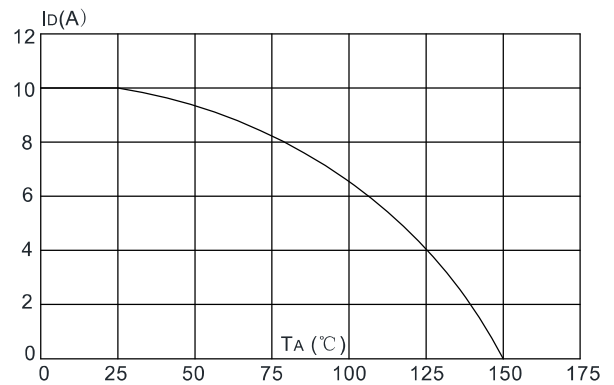
**Figure 8:** Normalized on Resistance vs. Junction Temperature



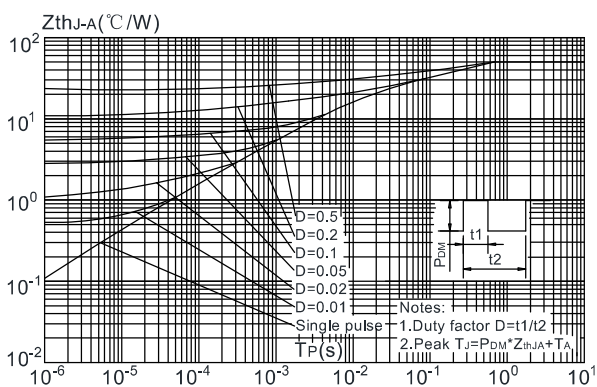
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



**AP50N04Q**  
N-Channel Enhancement Mosfet

**PDFN3X3-8L Package Information**

