

HRLD72N06

65V N-Channel Trench MOSFET

Features

- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% R_g Tested
- Lead free, Halogen Free

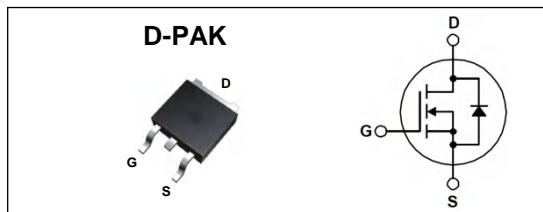
Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

Key Parameters

Parameter	Value	Unit
BV _{DSS}	65	V
I _D	73	A
R _{DS(on)} , max @10V	7.2	mΩ
R _{DS(on)} , max @4.5V	12.5	mΩ

Package & Internal Circuit



Absolute Maximum Ratings

T_J=25°C unless otherwise specified

Symbol	Parameter		Value	Units
V _{DSS}	Drain-Source Voltage		65	V
V _{GS}	Gate-Source Voltage		±20	V
I _D	Drain Current	T _C = 25°C	73	A
		T _C = 100°C	46	A
I _{DM}	Pulsed Drain Current		292	A
E _{AS}	Single Pulsed Avalanche Energy		12.5	mJ
P _D	Power Dissipation	T _C = 25°C	96	W
		T _A = 25°C	1.1	W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	--	1.3	°C/W
R _{θJA}	Junction-to-Ambient (steady state)	--	110	°C/W

Electrical Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0	--	2.5	V
$R_{DS(\text{ON})}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	--	6.0	7.2	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$	--	9.6	12.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$	--	10	--	S
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	65	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	1	μA
		$V_{DS} = 48 \text{ V}, T_J = 85^\circ\text{C}$	--	--	10	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	± 1	μA
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	--	1575	--	pF
C_{oss}	Output Capacitance		--	785	--	pF
C_{rss}	Reverse Transfer Capacitance		--	30	--	pF
R_g	Gate Resistance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V}, f = 1 \text{ MHz}$	--	1.25	--	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 30 \text{ V}, I_D = 10 \text{ A}, R_G = 10 \Omega$	--	15	--	ns
t_r	Turn-On Rise Time		--	21	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	136	--	ns
t_f	Turn-Off Fall Time		--	27	--	ns
Q_g	Total Gate Charge	$V_{DS} = 30 \text{ V}, I_D = 10 \text{ A}, V_{GS} = 10 \text{ V}$	--	38.5	--	nC
Q_{gs}	Gate-Source Charge		--	7.5	--	nC
Q_{gd}	Gate-Drain Charge		--	4.5	--	nC
Source-Drain Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 1 \text{ A}, V_{GS} = 0 \text{ V}$	--	0.9	1.2	V
trr	Reverse Recovery Time	$I_S = 10 \text{ A}, V_{GS} = 10 \text{ V}$ $dI_F/dt = 100 \text{ A}/\mu\text{s}$	--	48.4	--	ns
Qrr	Reverse Recovery Charge		--	54.2	--	nC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $I_{AS}=5\text{A}$, $V_{DD}=30\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

Typical Characteristics

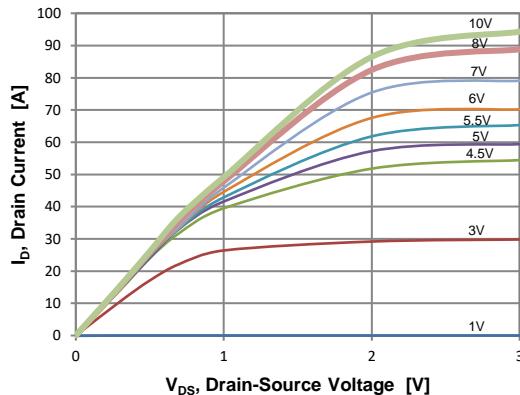


Figure 1. On Region Characteristics

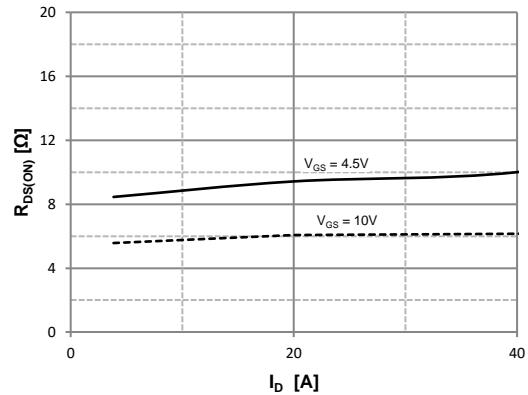


Figure 2. On Resistance Variation vs Drain Current and Gate Voltage

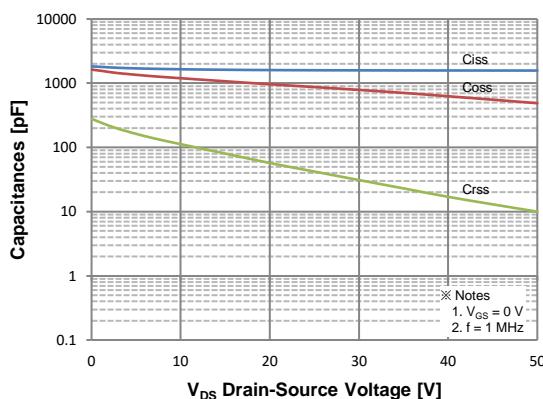


Figure 3. Capacitance Characteristics

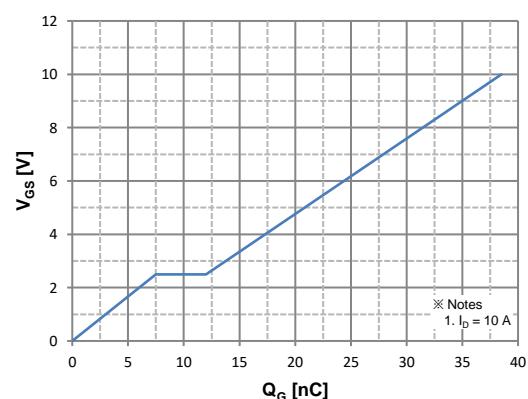


Figure 4. Gate Charge Characteristics

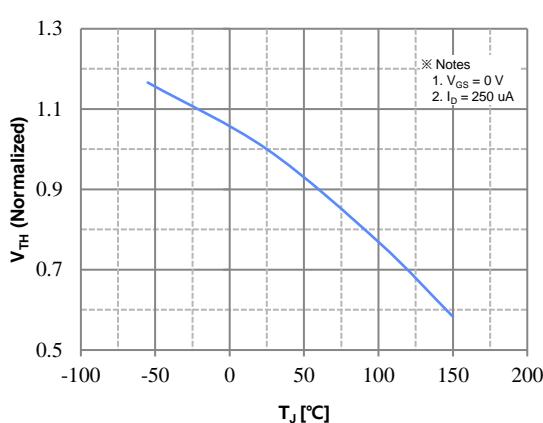


Figure 4. Gate Threshold Voltage vs Temperature

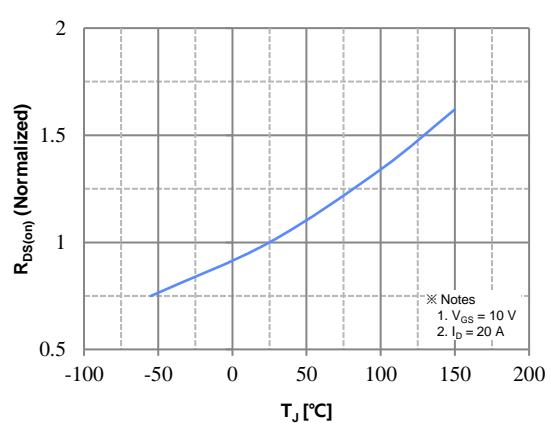


Figure 6. On-Resistance Variation vs Temperature

Typical Characteristics (continued)

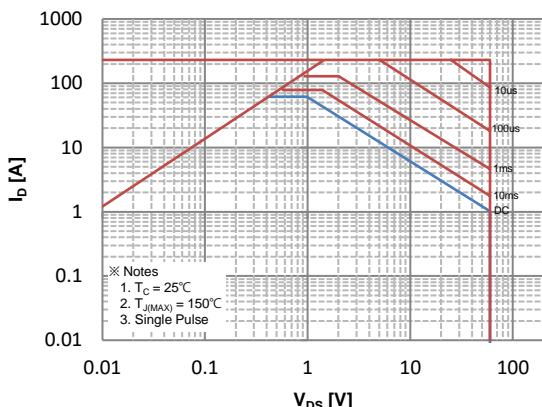


Figure 7. Maximum Safe Operating Area

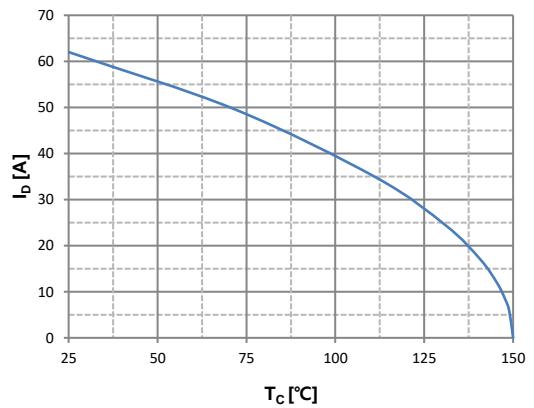


Figure 8. Maximum Drain Current vs Case Temperature

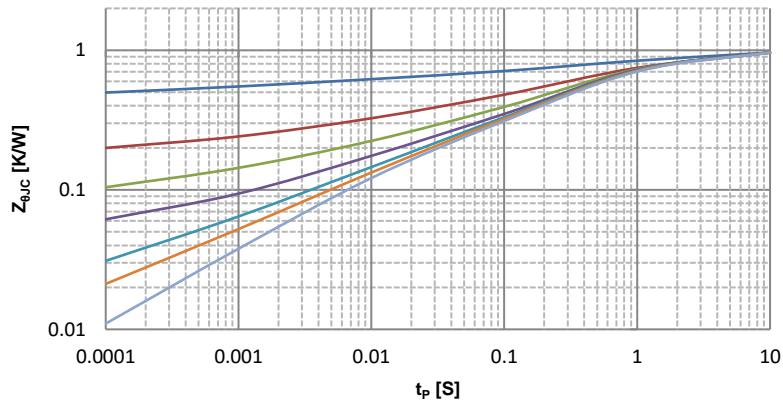


Figure 9. Transient Thermal Response Curve

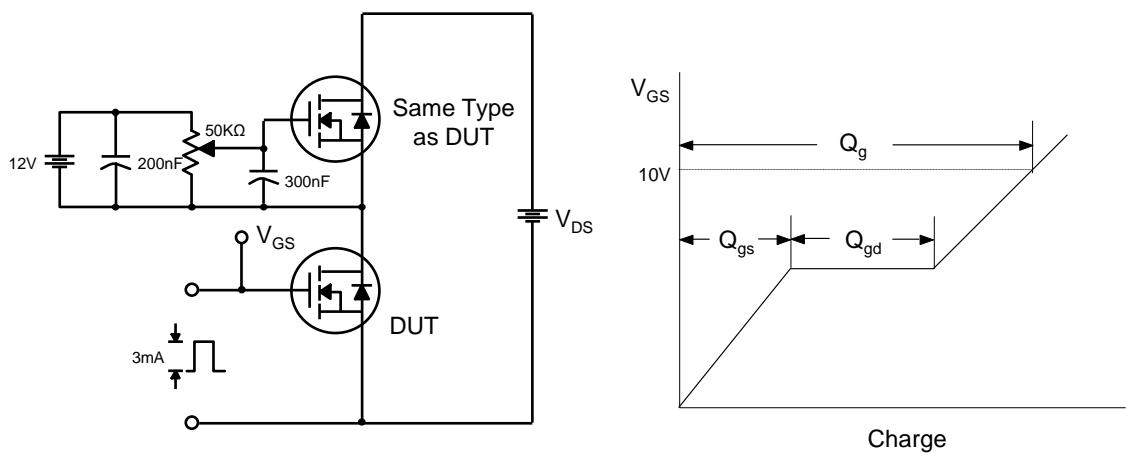
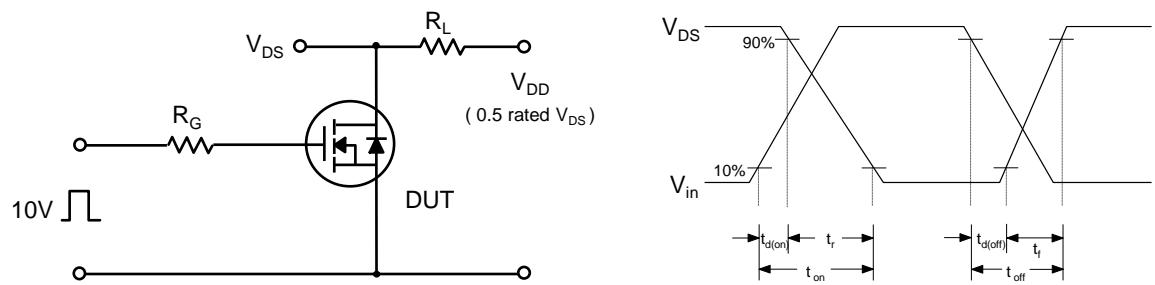
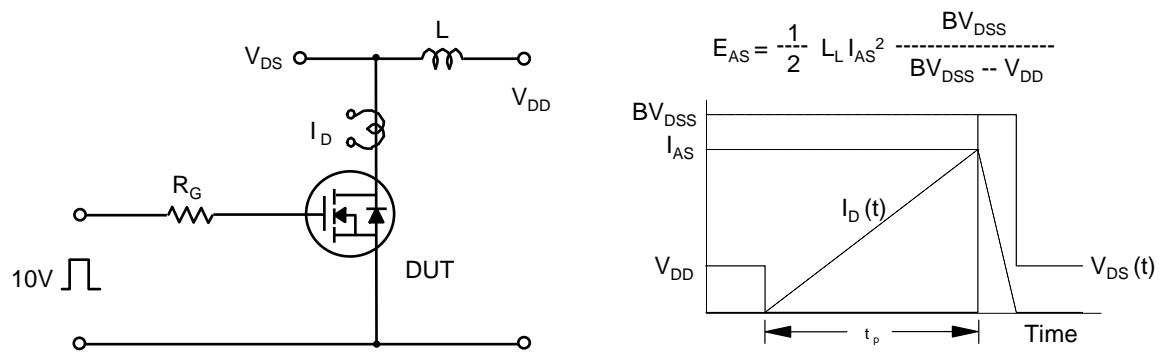
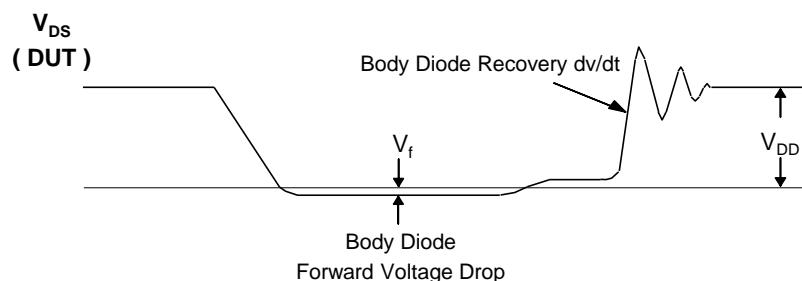
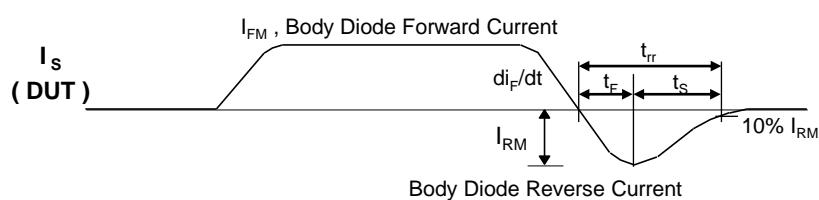
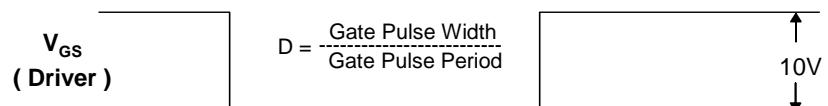
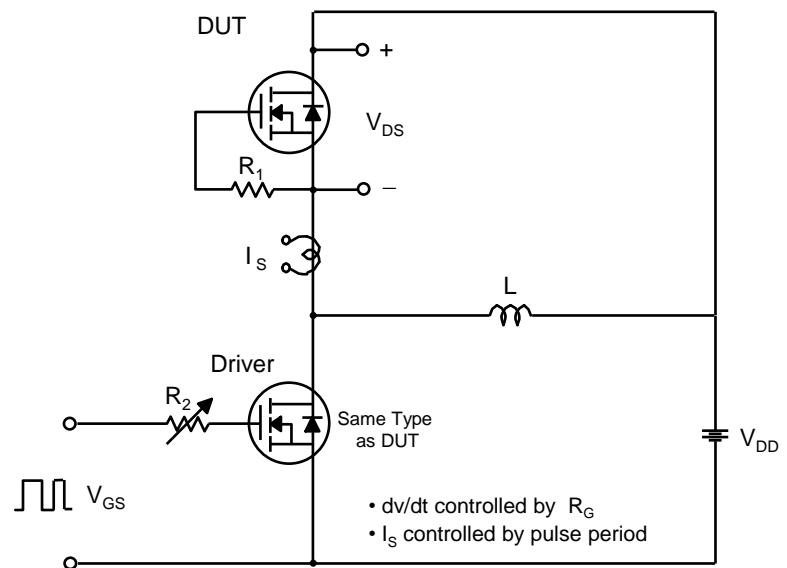
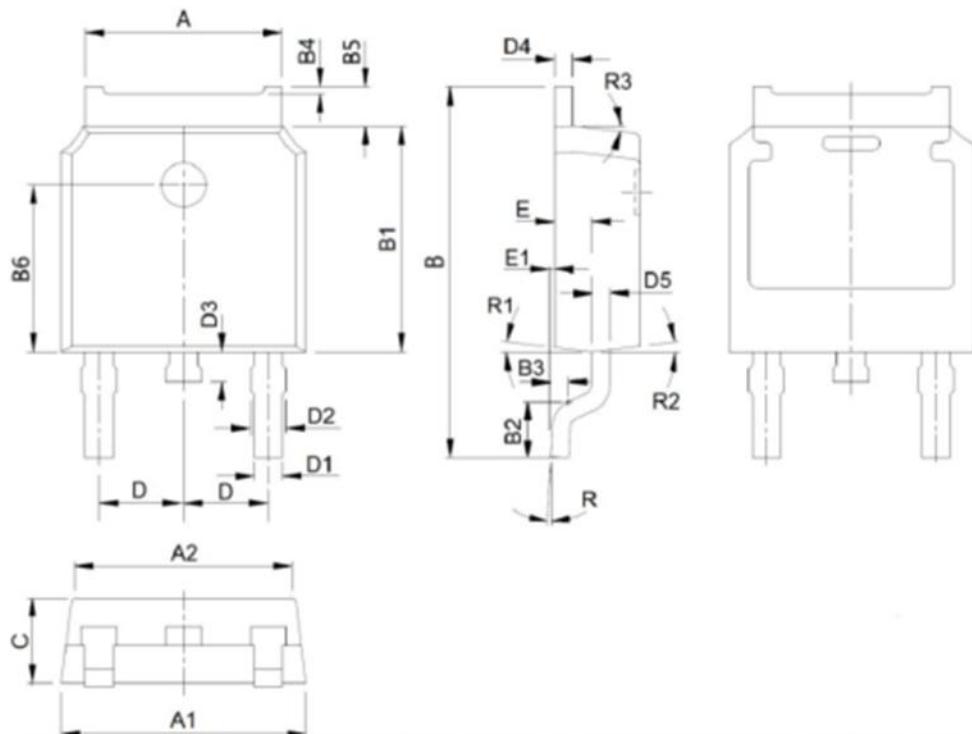
Fig 12. Gate Charge Test Circuit & Waveform**Fig 13. Resistive Switching Test Circuit & Waveforms****Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK
(TO-252A)

Symbol	Dimensions (mm)	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	5.3 ± 0.2	B5	0.95 ± 0.1	D5	0.5 ± 0.08
A1	6.6 ± 0.2	B6	4.5 ± 0.15	E	1.01 ± 0.15
A2	5.8 ± 0.2	C	2.3 ± 0.15	E1	0.1 ± 0.05
B	9.9 ± 0.4	D	2.286(typ.)	R	$3^\circ \pm 3^\circ$
B1	6.1 ± 0.2	D1	0.76 ± 0.1	R1	7° (typ.)
B2	1.5 ± 0.15	D2	0.91 ± 0.1	R2	7° (typ.)
B3	0.5 ± 0.1	D3	0.8 ± 0.15	R3	7° (typ.)
B4	0.1 (typ.)	D4	0.5 ± 0.08		

变更前	
D1	0.62 ± 0.15
D2	0.75 ± 0.15