

HRLO110N03K

30V N-Channel Trench MOSFET

Features

- ❑ Low Dense Cell Design, Logic Level
- ❑ Reliable and Rugged
- ❑ Advanced Trench Process Technology
- ❑ 100% UIS Tested, 100% Rg Tested
- ❑ Lead free, Halogen Free

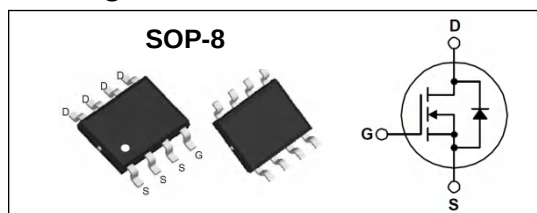
Application

- ❑ Power Management in Inverter System
- ❑ Synchronous Rectification

Key Parameters

Parameter	Value	Unit
BV_{DSS}	30	V
I_D	13.8	A
$R_{DS(on)}$, typ @10V	9.0	mΩ
$R_{DS(on)}$, typ @4.5V	13.0	mΩ

Package & Internal Circuit



Absolute Maximum Ratings $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	$T_A = 25^{\circ}\text{C}$	13.8	A
		$T_A = 100^{\circ}\text{C}$	8.7	A
I_{DM}	Pulsed Drain Current		55	A
E_{AS}	Single Pulsed Avalanche Energy	$L=1\text{mH}$	210	mJ
P_D	Power Dissipation	$T_A = 25^{\circ}\text{C}$	3.1	W
		$T_A = 70^{\circ}\text{C}$	2.0	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^{\circ}\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Lead	--	24	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient ($t \leq 10\text{s}$)	--	40	$^{\circ}\text{C/W}$
	Junction-to-Ambient (steady state)	--	75	$^{\circ}\text{C/W}$

Electrical Characteristics $T_J=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V _{GS}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.0	--	3.0	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 13 A	--	9.0	11.0	mΩ
		V _{GS} = 4.5 V, I _D = 10 A	--	13.0	15.6	mΩ
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	30	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 24 V, T _J = 125 °C	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	--	--	±100	nA
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	--	1170	--	pF
C _{oss}	Output Capacitance		--	165	--	pF
C _{rss}	Reverse Transfer Capacitance		--	105	--	pF
R _g	Gate Resistance	V _{GS} = 0 V, V _{DS} = 0 V, f = 1MHz	--	1	--	Ω
Switching Characteristics						
t _{d(on)}	Turn-On Time	V _{DS} = 15 V, I _D = 13 A, R _G = 6 Ω	--	12	--	ns
t _r	Turn-On Rise Time		--	10	--	ns
t _{d(off)}	Turn-Off Delay Time		--	55	--	ns
t _f	Turn-Off Fall Time		--	15	--	ns
Q _{g(10V)}	Total Gate Charge	V _{DS} = 24 V, I _D = 13 A, V _{GS} = 10 V	--	21	--	nC
Q _{g(4.5V)}	Total Gate Charge		--	10	--	nC
Q _{gs}	Gate-Source Charge		--	5.4	--	nC
Q _{gd}	Gate-Drain Charge		--	2.8	--	nC
Source-Drain Diode Characteristics						
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 13 A, V _{GS} = 0 V	--	--	1.3	V
trr	Reverse Recovery Time	I _S = 20 A, V _{GS} = 0 V di _F /dt = 100 A/μs	--	23	--	ns
Qrr	Reverse Recovery Charge		--	15	--	nC

Typical Characteristics

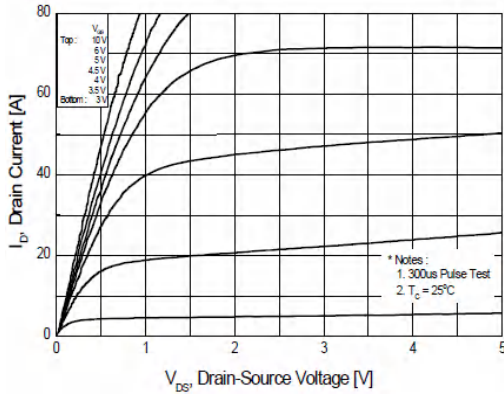


Figure 1. On Region Characteristics

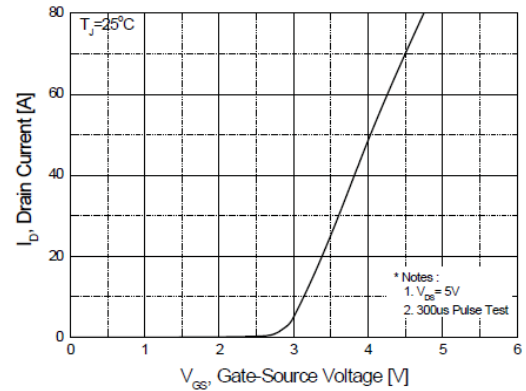


Figure 2. Transfer Characteristics

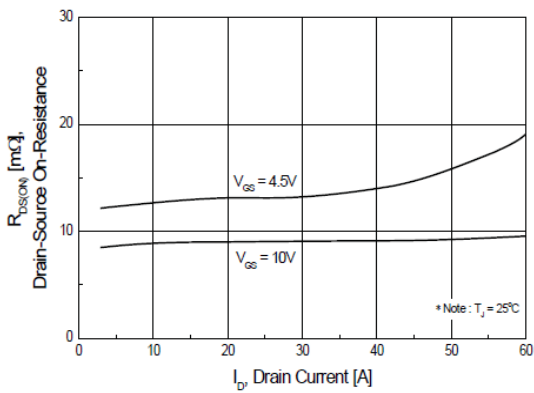


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

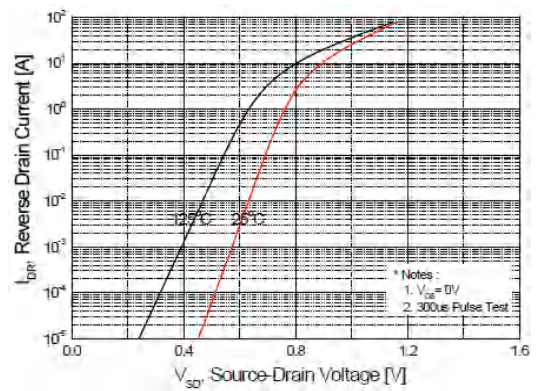


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

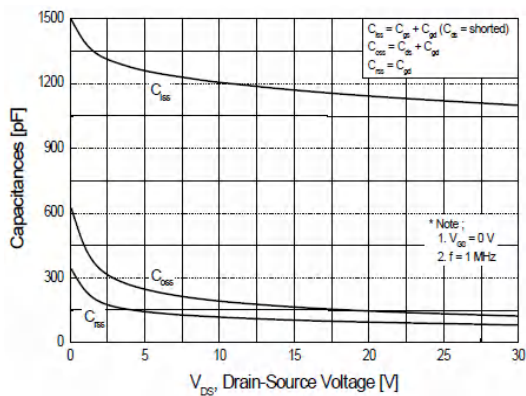


Figure 5. Capacitance Characteristics

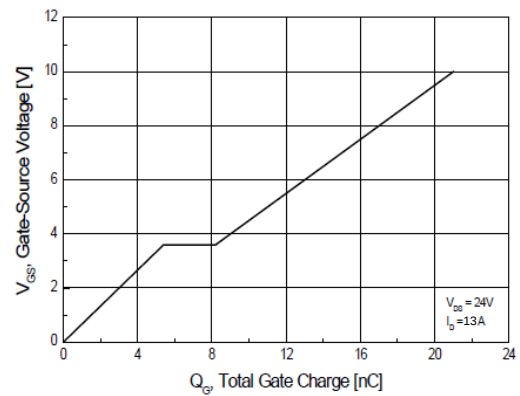


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

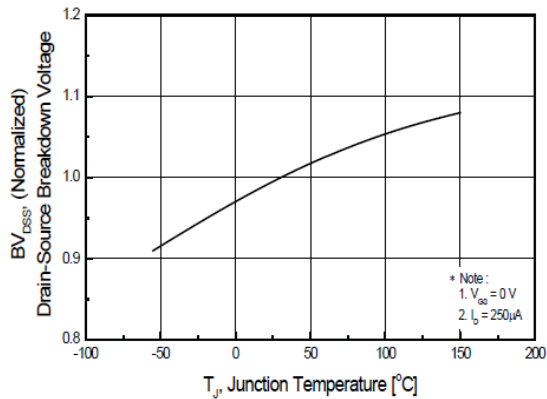


Figure 7. On-Resistance Variation vs Gate-Source Voltage

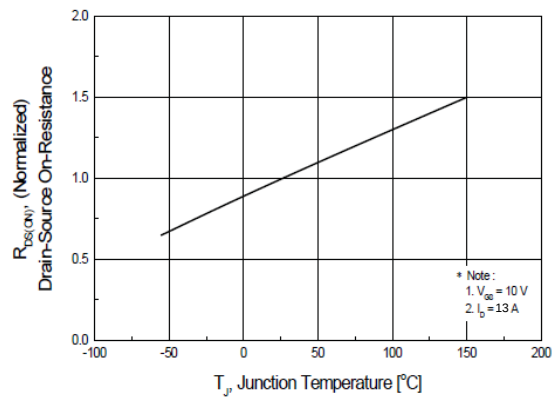


Figure 8. On-Resistance Variation vs Temperature

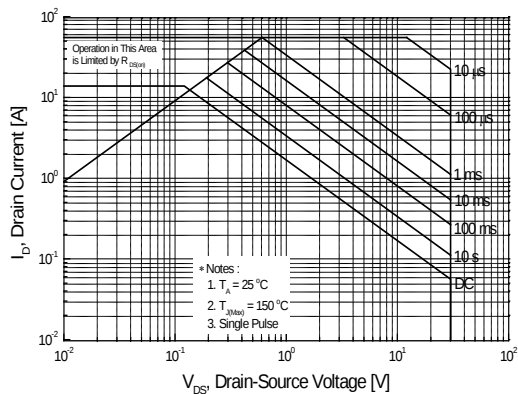


Figure 9. Maximum Safe Operating Area

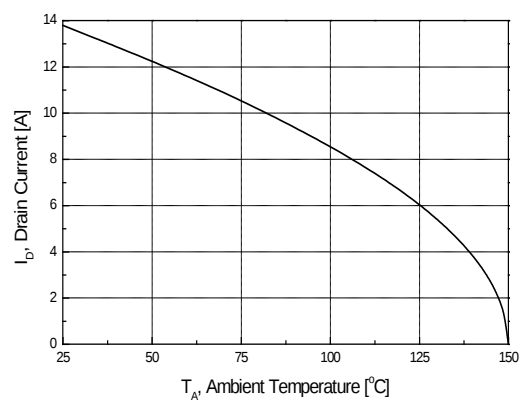


Figure 10. Maximum Drain Current vs Case Temperature

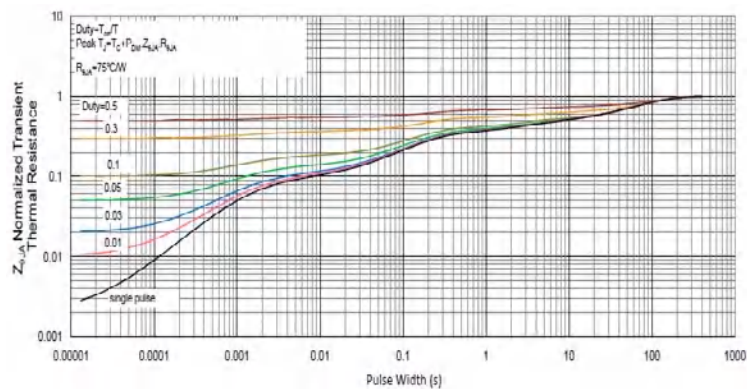


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

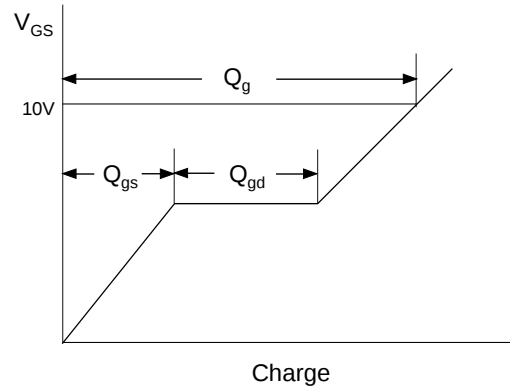
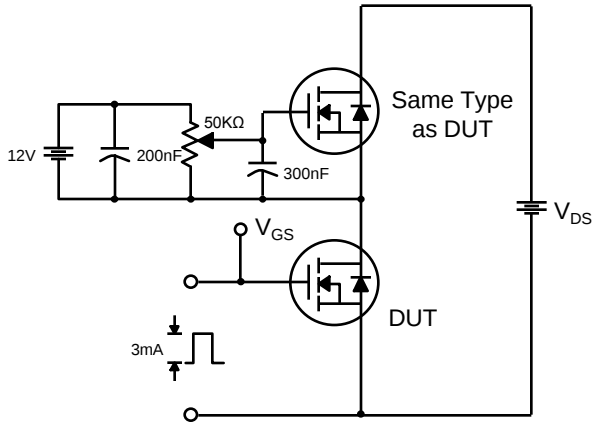


Fig 13. Resistive Switching Test Circuit & Waveforms

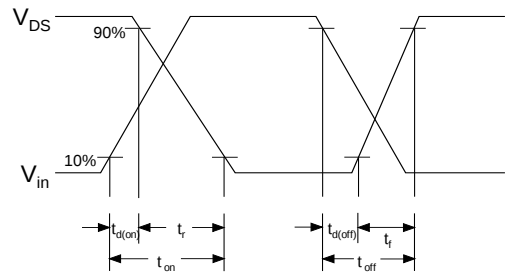
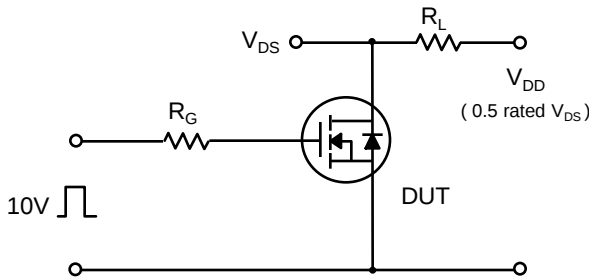


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

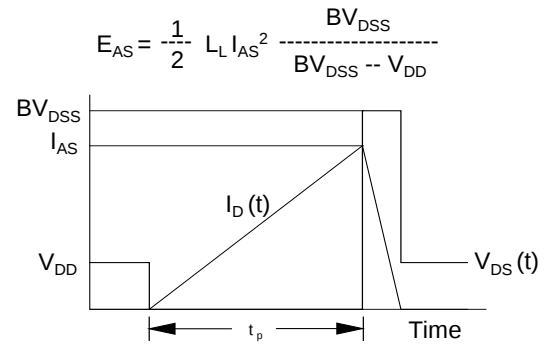
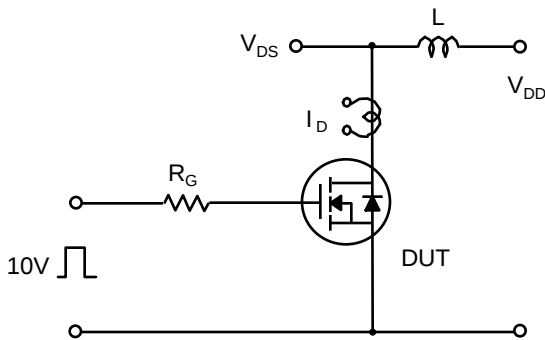
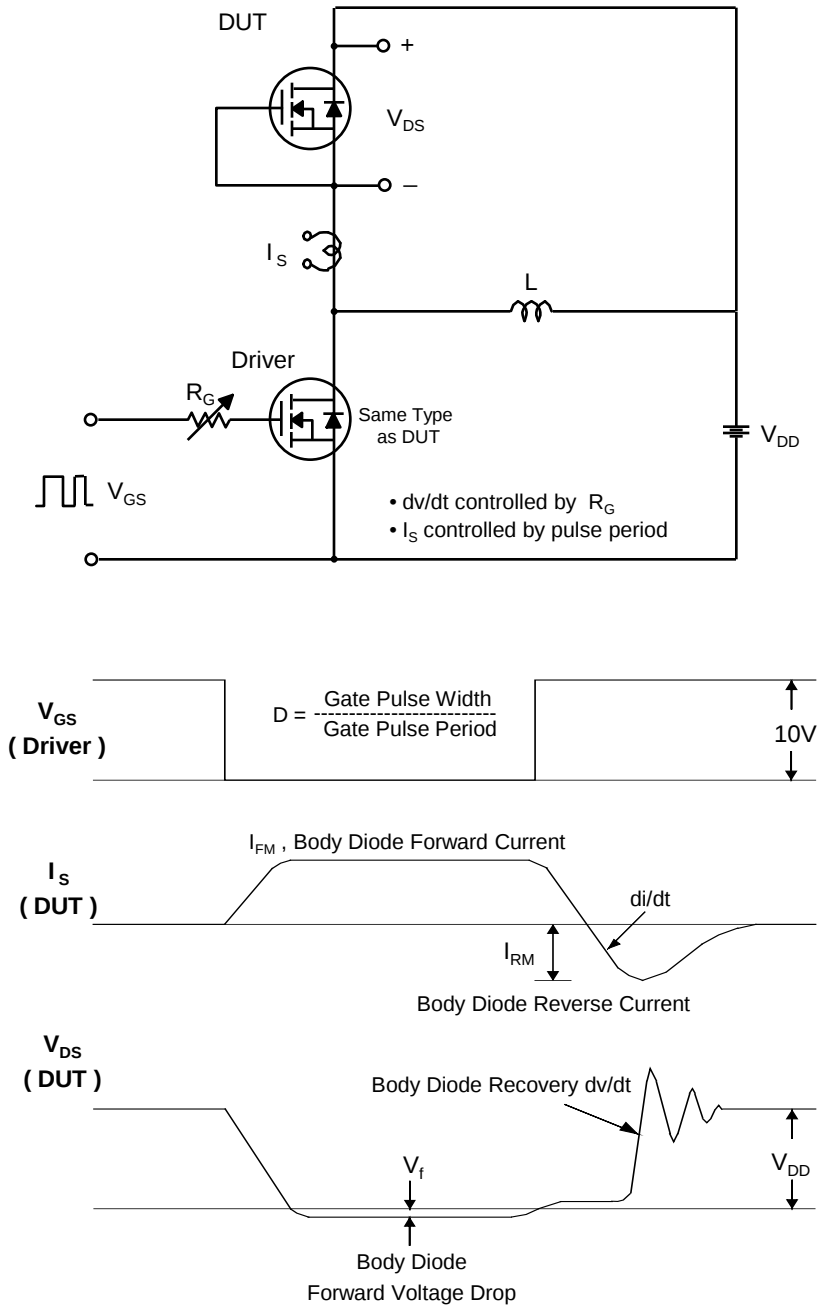


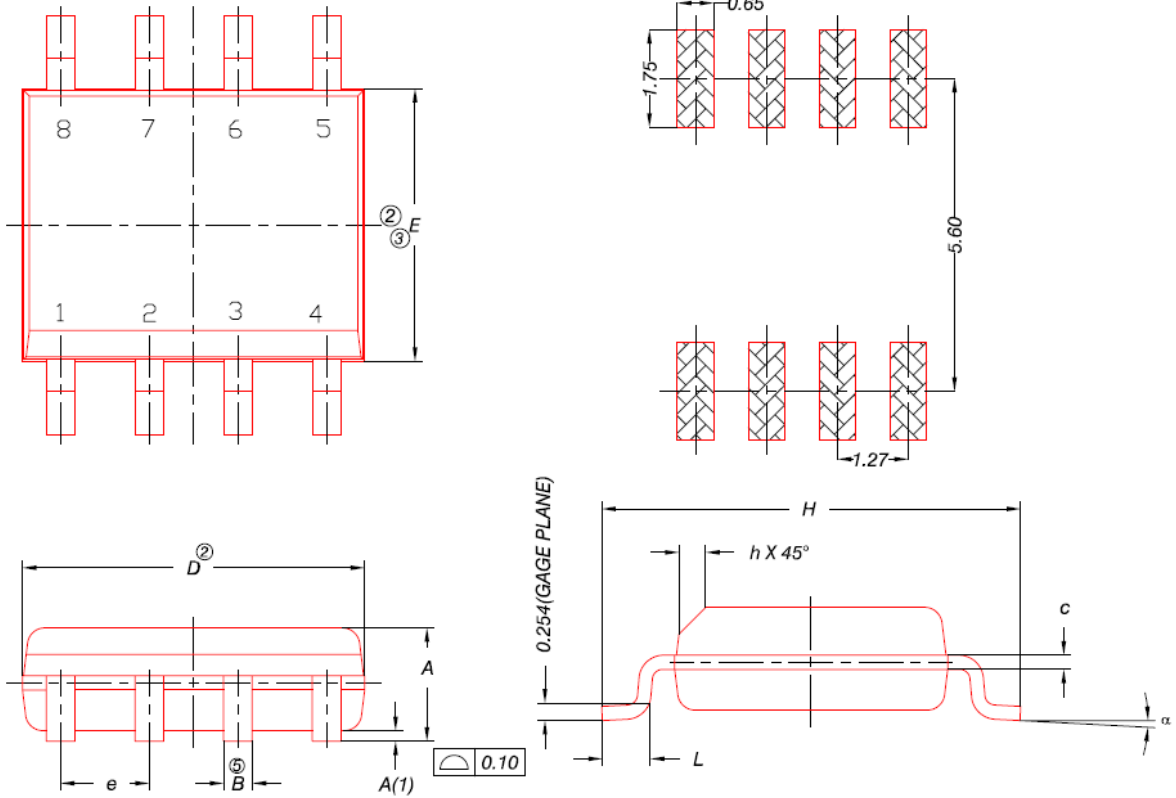
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

SOP-8

*Land Pattern
(Only for Reference)*



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A(1)	0.10	0.18	0.25
B	0.38	0.45	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
H	5.80	6.00	6.20
L	0.50	0.72	0.93
α	0°	4°	8°
h	0.25	0.38	0.50