

HRLFS136N10P

100V N-Channel Trench MOSFET

Features

- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead free, Halogen Free

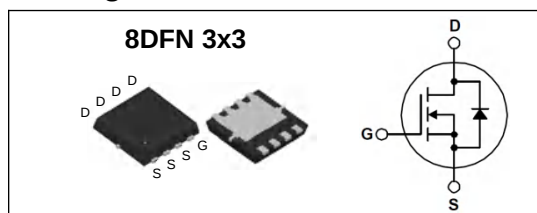
Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

Key Parameters

Parameter	Value	Unit
BV_{DSS}	100	V
I_D	48	A
$R_{DS(on)}$, typ @10V	11.3	m Ω
$R_{DS(on)}$, typ @4.5V	16.7	m Ω

Package & Internal Circuit



Absolute Maximum Ratings $T_J=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	$T_C = 25^{\circ}\text{C}$	48	A
		$T_C = 100^{\circ}\text{C}$	30	A
I_{DM}	Pulsed Drain Current		192	A
E_{AS}	Single Pulsed Avalanche Energy	$L=1\text{mH}$	60	mJ
V_{SPIKE}	V_{DS} Spike	10us	120	V
P_D	Power Dissipation	$T_C = 25^{\circ}\text{C}$	61	W
		$T_A = 25^{\circ}\text{C}$	2.0	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^{\circ}\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	2.04	$^{\circ}\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (steady state)	--	62	$^{\circ}\text{C/W}$

Electrical Characteristics $T_J=25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
On Characteristics						
V _{GS}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.0	--	2.5	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 20 A	--	11.3	13.6	mΩ
		V _{GS} = 4.5 V, I _D = 15 A	--	16.7	22.0	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 3 A	--	8	--	S
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	100	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 100 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 80 V, T _J = 85°C	--	--	10	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	--	--	±100	nA
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1.0 MHz	--	1640	--	pF
C _{oss}	Output Capacitance		--	240	--	pF
C _{rss}	Reverse Transfer Capacitance		--	4	--	pF
R _g	Gate Resistance	V _{GS} = 0 V, V _{DS} = 0 V, f = 1MHz	--	1.2	--	Ω
Switching Characteristics						
t _{d(on)}	Turn-On Time	V _{DS} = 50 V, I _D = 10 A, R _G = 6 Ω	--	14.2	--	ns
t _r	Turn-On Rise Time		--	20.8	--	ns
t _{d(off)}	Turn-Off Delay Time		--	42	--	ns
t _f	Turn-Off Fall Time		--	30	--	ns
Q _g	Total Gate Charge	V _{DS} = 50 V, I _D = 10 A, V _{GS} = 10 V	--	27.8	--	nC
Q _{gs}	Gate-Source Charge		--	3.5	--	nC
Q _{gd}	Gate-Drain Charge		--	8.8	--	nC
Source-Drain Diode Characteristics						
V _{SD}	Source-Drain Diode Forward Voltage	I _S = 1 A, V _{GS} = 0 V	--	--	1.0	V
trr	Reverse Recovery Time	I _S = 10 A, V _{GS} = 10 V di _F /dt = 100 A/μs	--	43.5	--	ns
Qrr	Reverse Recovery Charge		--	59.6	--	nC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=1\text{ mH}, I_{AS}=11\text{ A}, V_{DD}=50\text{ V}, R_G=25\text{ }\Omega$, Starting $T_J=25^{\circ}\text{C}$

Typical Characteristics

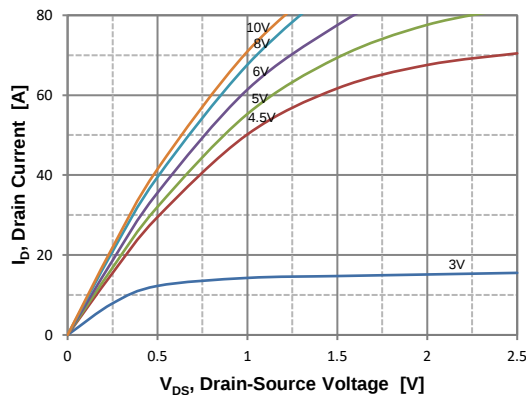


Figure 1. On Region Characteristics

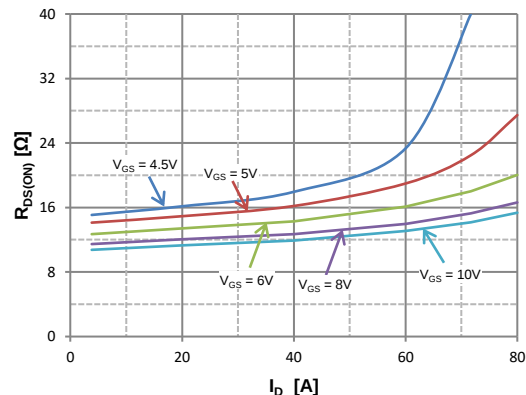


Figure 2. On Resistance Variation vs Drain Current and Gate Voltage

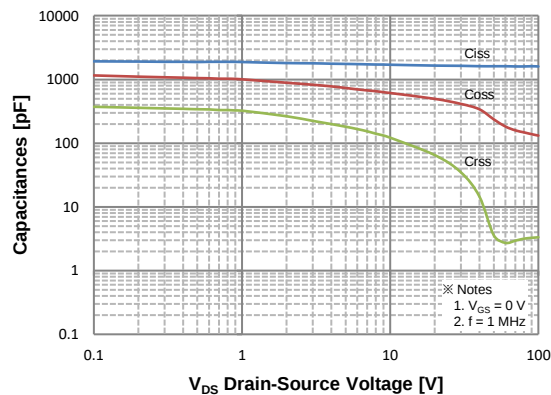


Figure 3. Capacitance Characteristics

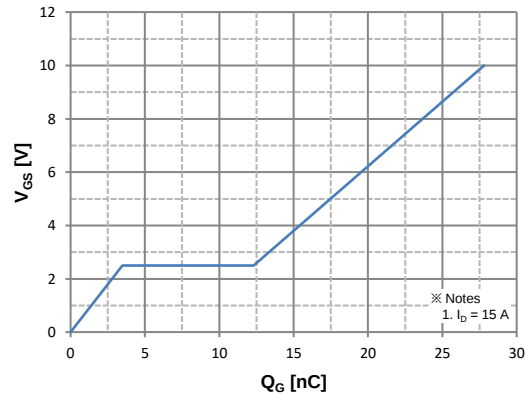


Figure 4. Gate Charge Characteristics

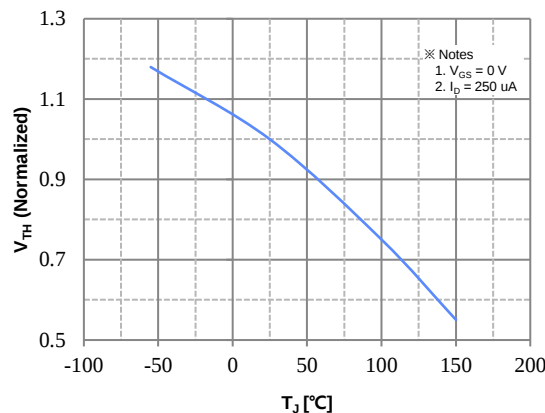


Figure 4. Gate Threshold Voltage vs Temperature

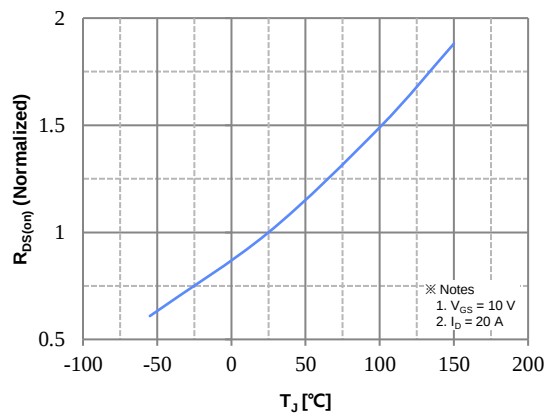


Figure 6. On-Resistance Variation vs Temperature

Typical Characteristics (continued)

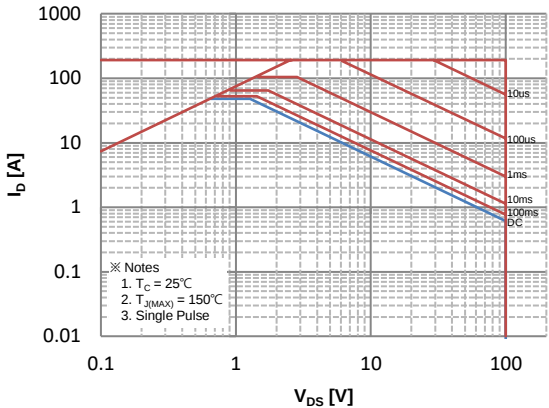


Figure 7. Maximum Safe Operating Area

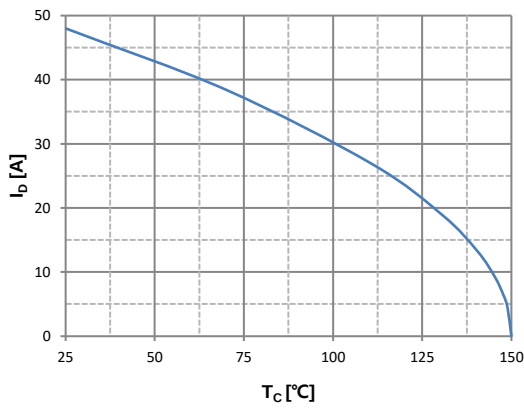


Figure 8. Maximum Drain Current vs Case Temperature

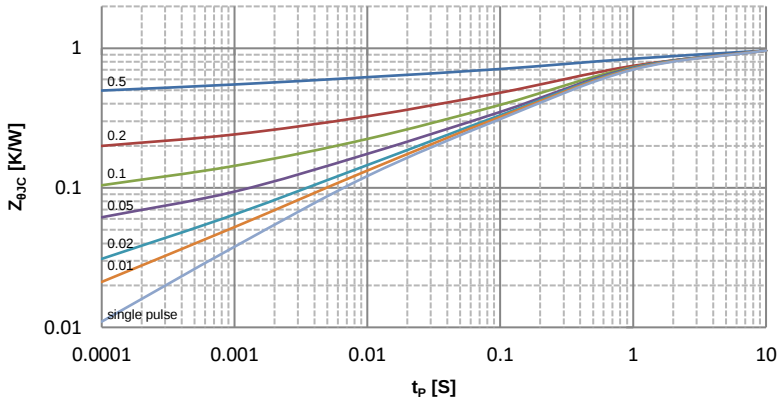


Figure 9. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

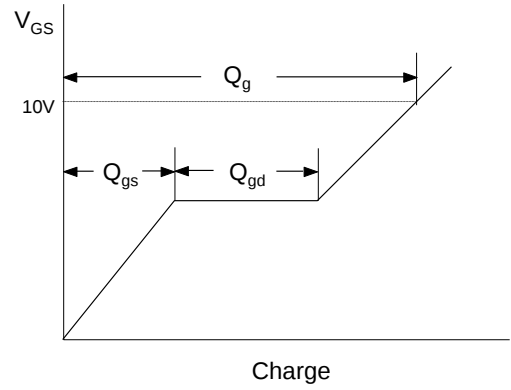
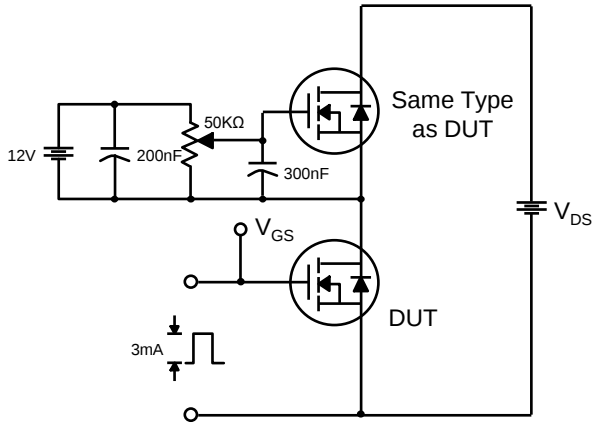


Fig 13. Resistive Switching Test Circuit & Waveforms

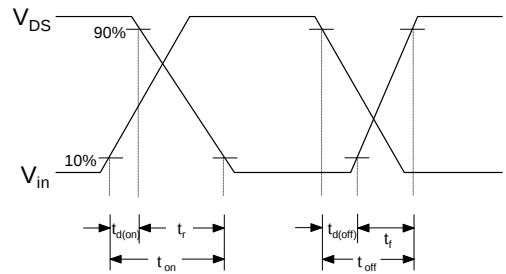
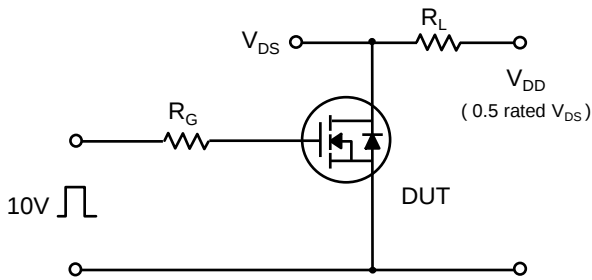


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

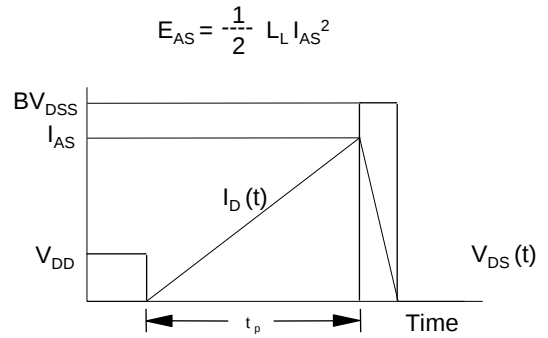
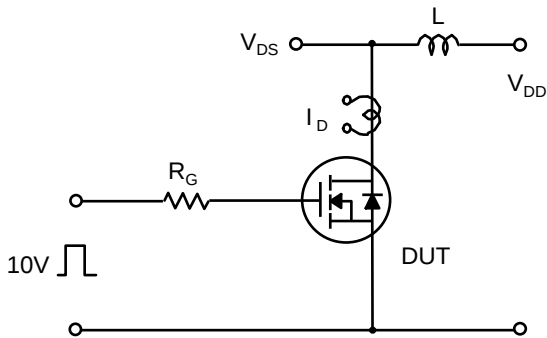
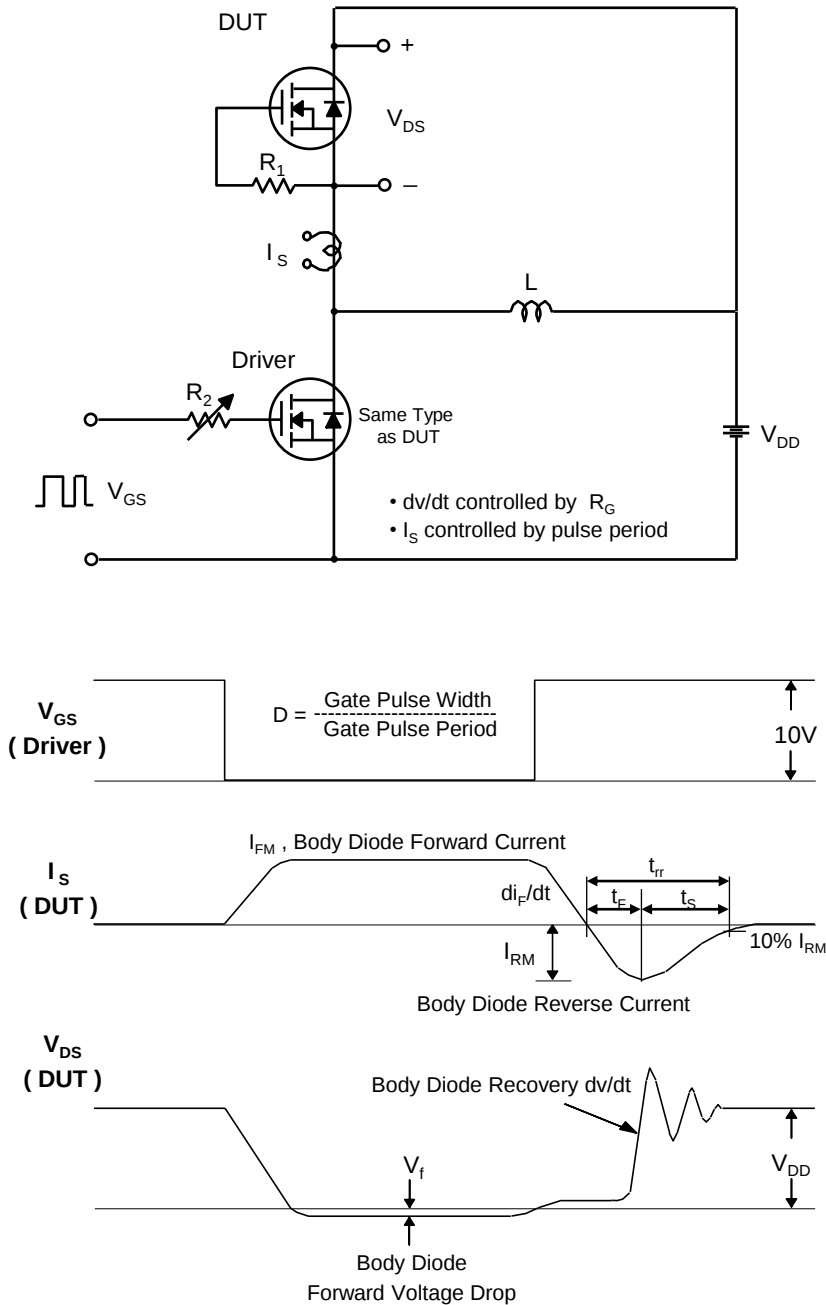
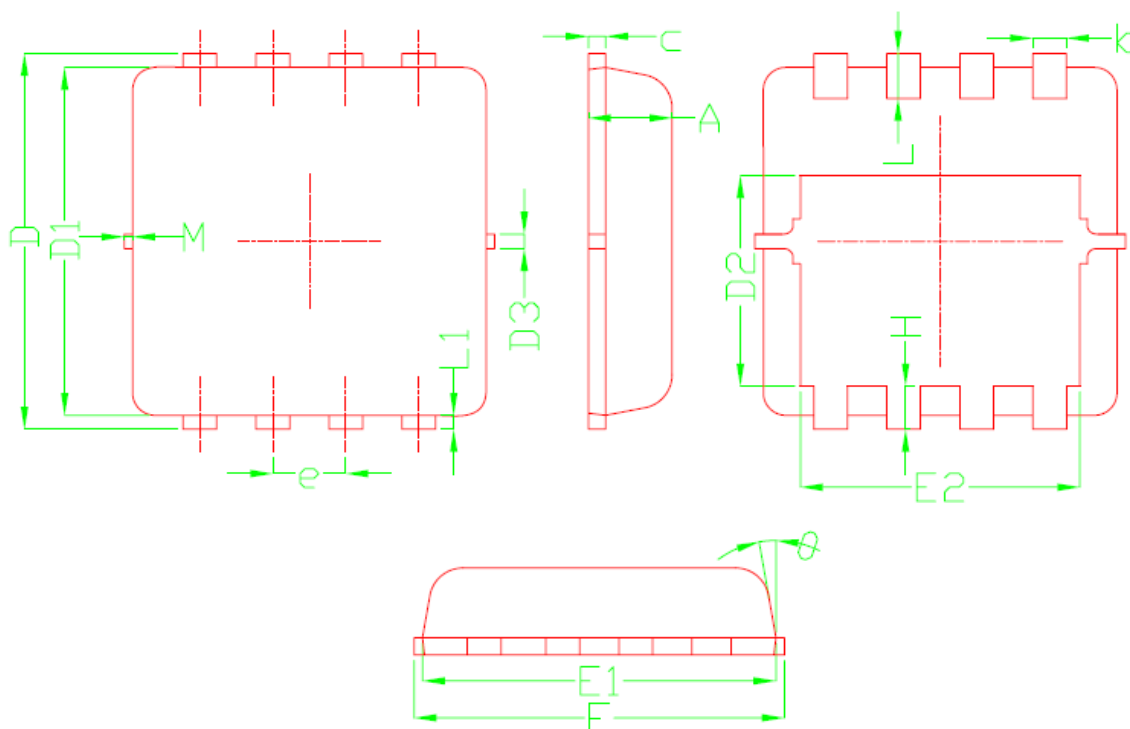


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

8DFN 3x3



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
<i>A</i>	0.70	0.75	0.80
<i>b</i>	0.25	0.30	0.35
<i>c</i>	0.10	0.15	0.25
<i>D</i>	3.25	3.35	3.45
<i>D1</i>	3.00	3.10	3.20
<i>D2</i>	1.78	1.88	1.98
<i>D3</i>	---	0.13	---
<i>E</i>	3.20	3.30	3.40
<i>E1</i>	3.00	3.15	3.20
<i>E2</i>	2.39	2.49	2.59
<i>e</i>	0.65BSC		
<i>H</i>	0.30	0.39	0.50
<i>L</i>	0.30	0.40	0.50
<i>L1</i>	---	0.13	---
θ	---	10°	12°
<i>M</i>	*	*	0.15
* Not specified			

Land Pattern
(Only for Reference)

