

# HCD65R1K0

## 650V N-Channel Super Junction MOSFET

### Features

- Very Low FOM ( $R_{DS(on)} \times Q_g$ )
- Extremely low switching loss
- Excellent stability and uniformity
- 100% Avalanche Tested
- Built-in ESD Diode

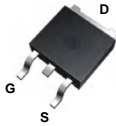
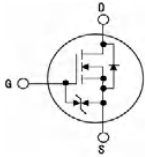
### Application

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)
- TV power & LED Lighting Power
- AC to DC Converters
- Telecom

### Key Parameters

Parameter	Value	Unit
$BV_{DSS} @ T_{j,max}$	700	V
$I_D$	4.8	A
$R_{DS(on), max}$	1.0	$\Omega$
$Q_g, Typ$	9.3	nC

### Package & Internal Circuit

D-PAK	SYMBOL
	

### Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain-Source Voltage	650	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	4.8	A
	Drain Current - Continuous ( $T_C = 100^\circ\text{C}$ )	3.0	A
$I_{DM}^{1)}$	Drain Current - Pulsed	14.4	A
$E_{AS}^{2)}$	Single Pulsed Avalanche Energy	43	mJ
$I_{AR}$	Avalanche Current	1.0	A
dv/dt	MOSFET dv/dt ruggedness, $V_{DS}=0\dots 400\text{V}$	50	V/ns
dv/dt	Reverse diode dv/dt, $V_{DS}=0\dots 400\text{V}$ , $I_{DS}\leq I_D$	15	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	50	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Resistance Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>On Characteristics</b>						
$V_{GS}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 140 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 1.3 \text{ A}$	-	0.87	1.0	$\Omega$
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0$	-	-	1	$\mu\text{A}$
		$V_{DS} = 650 \text{ V}, T_C = 150^\circ\text{C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 400 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$	-	390	-	pF
$C_{oss}$	Output Capacitance		-	13	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	2.1	-	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 325 \text{ V}, I_D = 1.8 \text{ A},$ $R_G = 25 \Omega$  (Note 3,4)	-	20	-	ns
$t_r$	Turn-On Rise Time		-	18	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	54	-	ns
$t_f$	Turn-Off Fall Time		-	19	-	ns
$Q_{gt}$	Total Gate Charge	$V_{DS} = 520 \text{ V}, I_D = 1.8 \text{ A},$ $V_{GS} = 10 \text{ V}$  (Note 3,4)	-	9.3	-	nC
$Q_{gs}$	Gate-Source Charge		-	1.8	-	nC
$Q_{gd}$	Gate-Drain Charge		-	3.0	-	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		-	-	4.8	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		-	-	14.4	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 1.8 \text{ A}$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_R = 400 \text{ V}, I_F = 1.8 \text{ A}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$	-	210	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	1.2	-	$\mu\text{C}$

**Notes :**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{AS}=1.0\text{A}$   $V_{DD}=50\text{V}$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
3. Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
4. Essentially Independent of Operating Temperature

# Typical Characteristics

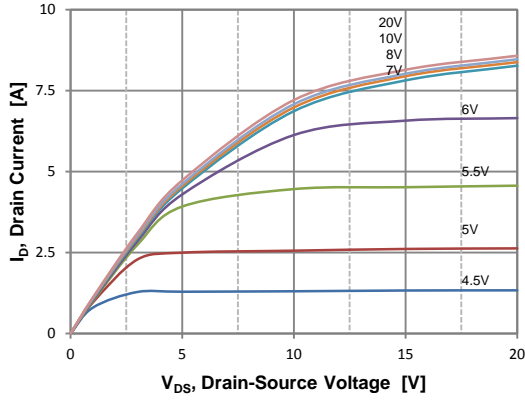


Figure 1. On Region Characteristics

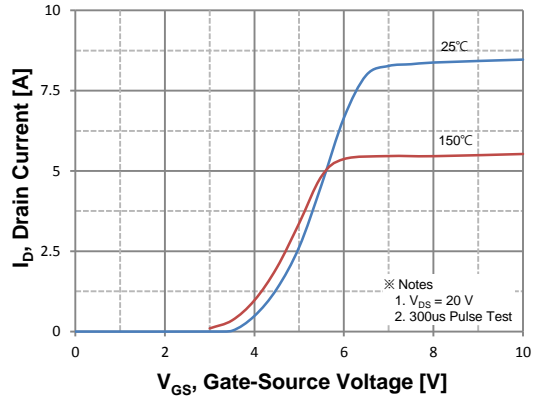


Figure 2. Transfer Characteristics

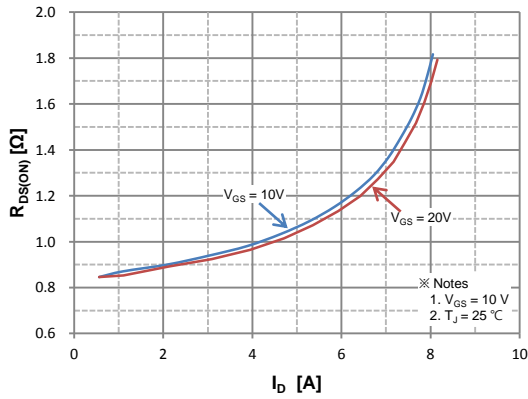


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

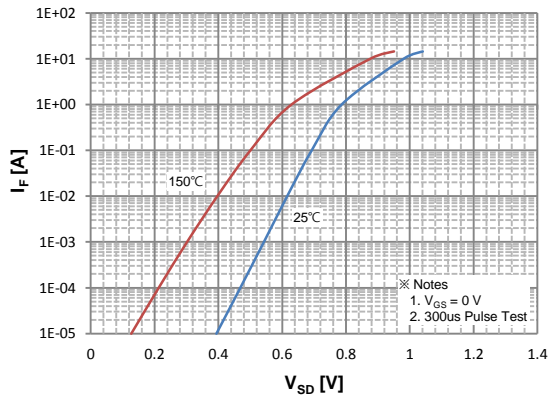


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

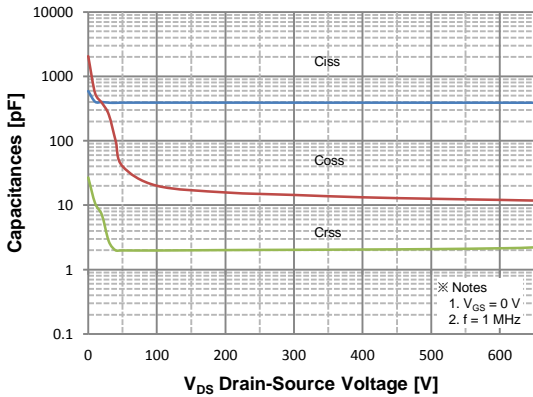


Figure 5. Capacitance Characteristics

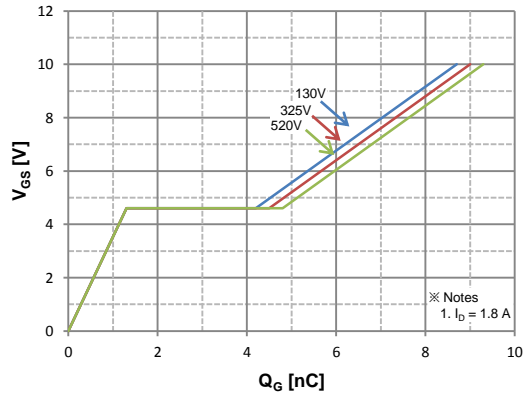


Figure 6. Gate Charge Characteristics

Typical Characteristics



Figure 7. Breakdown Voltage Variation vs. Temperature

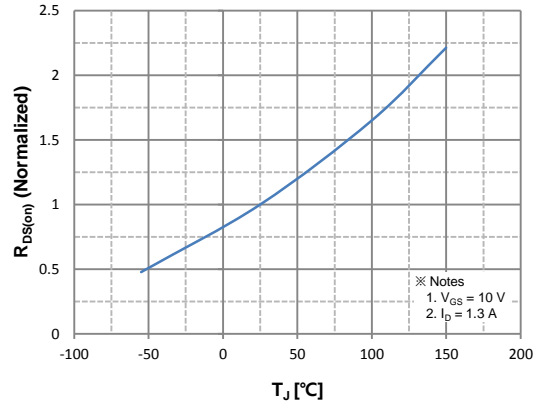


Figure 8. On-Resistance Variation vs. Temperature

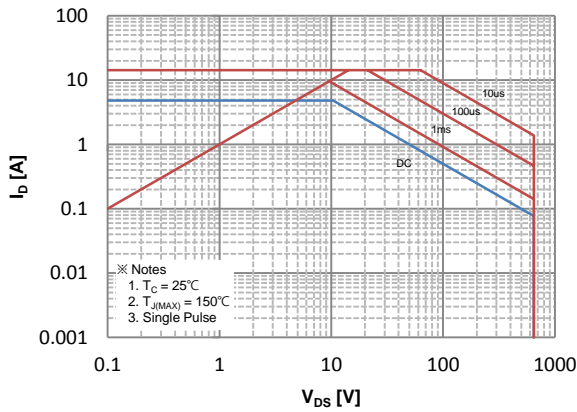


Figure 9. Maximum Safe Operating Area

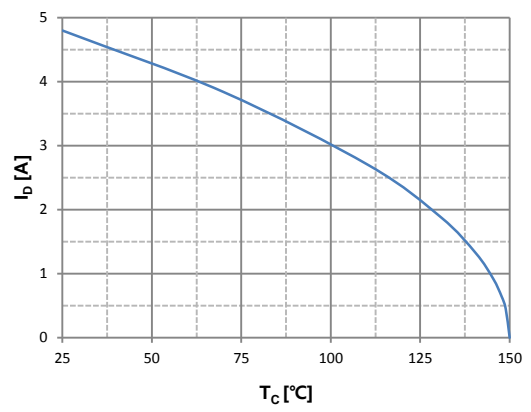


Figure 10. Maximum Drain Current vs. Case Temperature

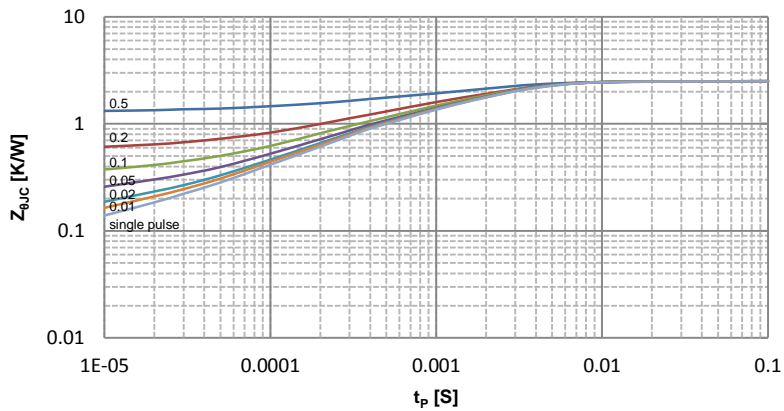


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform



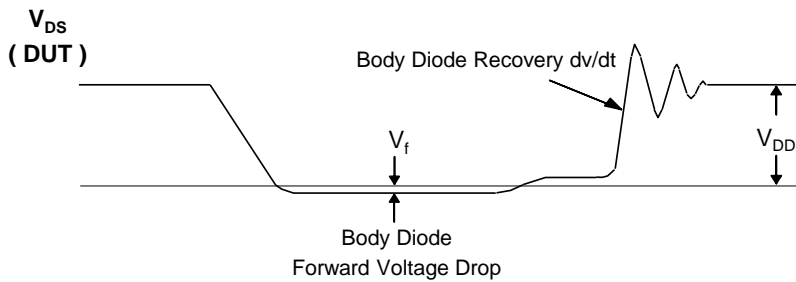
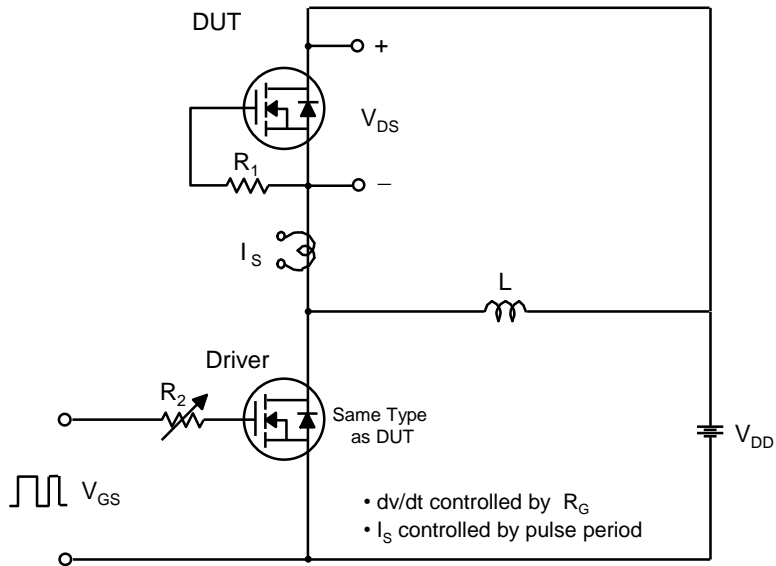
Fig 13. Resistive Switching Test Circuit & Waveforms



Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

D-PAK  
(TO-252A)

